NOTE:
SYNC AND DATA PULSES CONSIST OF TWO CYCLES OF A 1500-CPS TONE.

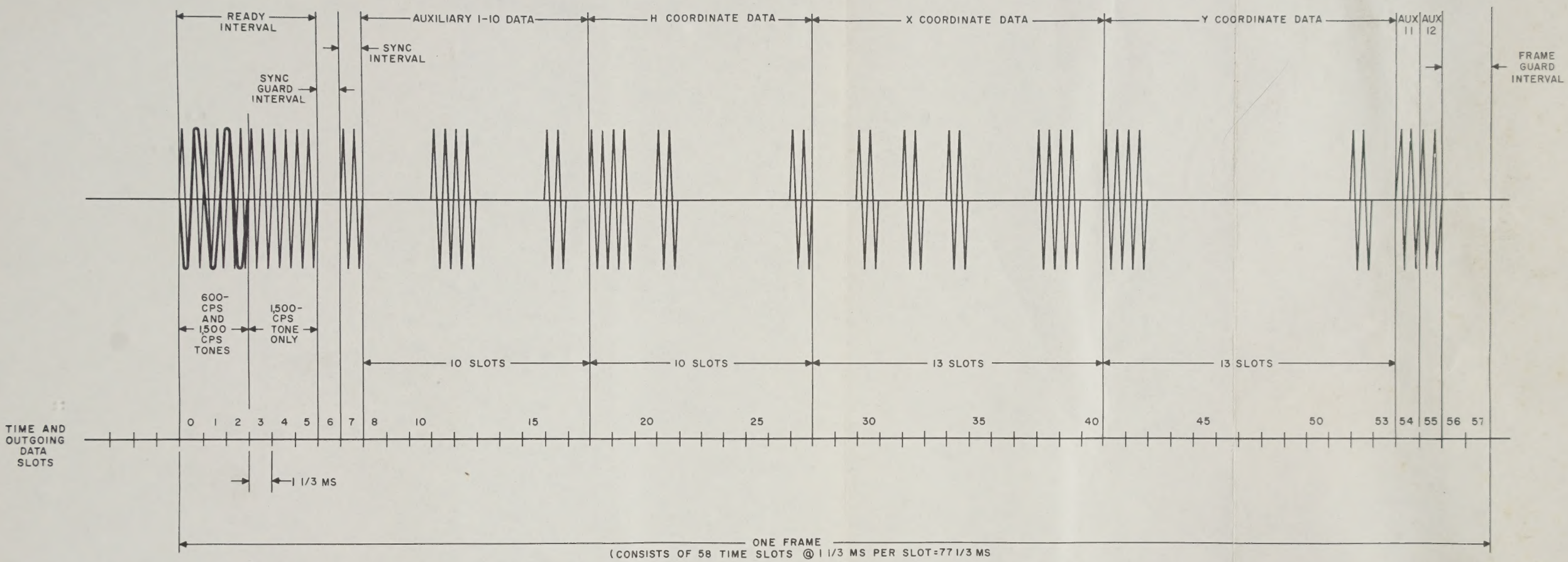
READY INTERVAL
AUXILIARY 1-10 DATA
H COORDINATE DATA
X COORDINATE DATA
Y COORDINATE DATA
AUX 11
AUX 12
SYNC INTERVAL
SYNC GUARD INTERVAL
FRAME GUARD INTERVAL
600-CPS AND 1,500 CPS TONES
1,500-CPS TONE ONLY
10 SLOTS
10 SLOTS
13 SLOTS
13 SLOTS
TIME AND OUTGOING DATA SLOTS
0 1 2 3 4 5 6 7 8 10 15 20 25 30 35 40 45 50 53 54 55 56 57
1 1/3 MS
ONE FRAME
(CONSISTS OF 58 TIME SLOTS @ 1 1/3 MS PER SLOT=77 1/3 MS

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Figure 2. Typical cycle of transmitted message.

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https://archive.org/details/tm11584021935tsq00unse

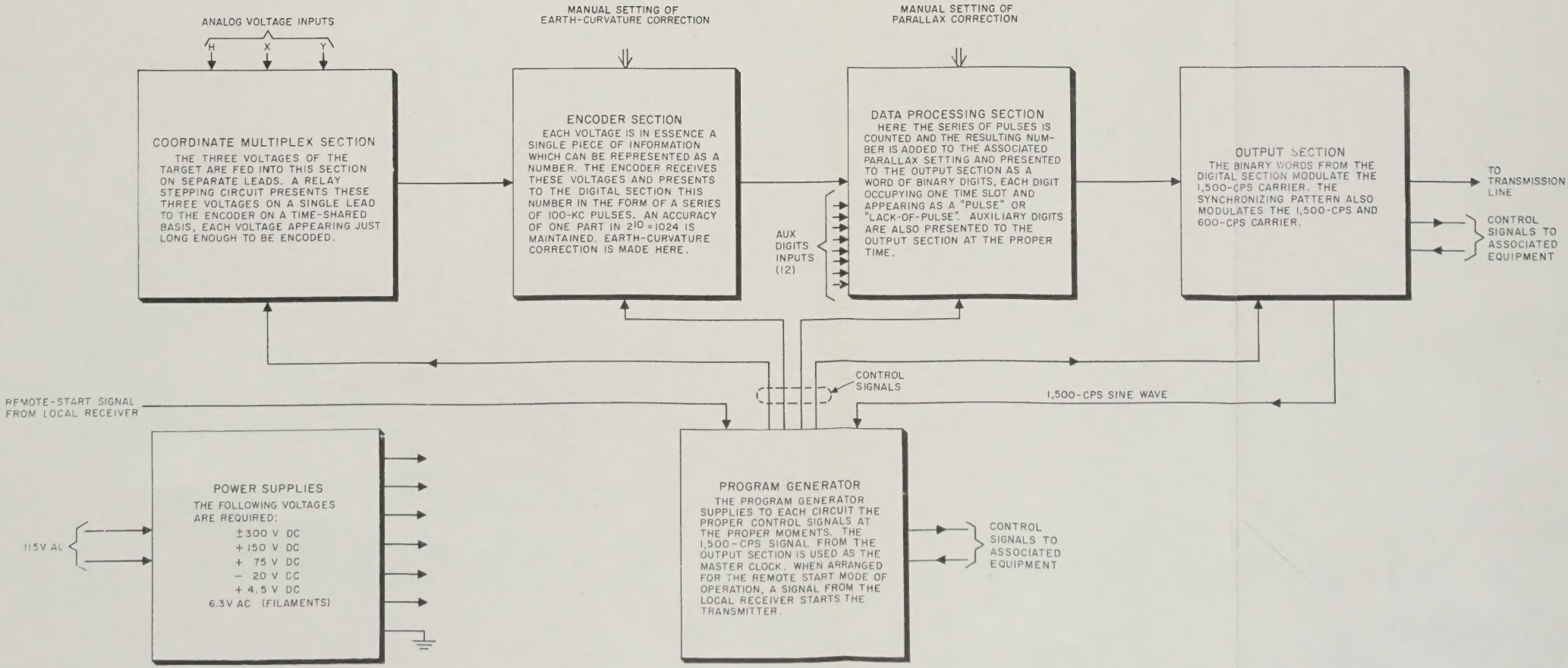
ANALOG VOLTAGE INPUTS
H
X
Y
COORDINATE MULTIPLEX SECTION
THE THREE VOLTAGES OF THE TARGET ARE FED INTO THIS SECTION ON SEPARATE LEADS. A RELAY STEPPING CIRCUIT PRESENTS THESE THREE VOLTAGES ON A SINGLE LEAD TO THE ENCODER ON A TIME-SHARED BASIS, EACH VOLTAGE APPEARING JUST LONG ENOUGH TO BE ENCODED.
MANUAL SETTING OF EARTH-CURVATURE CORRECTION
ENCODER SECTION
EACH VOLTAGE IS IN ESSENCE A SINGLE PIECE OF INFORMATION WHICH CAN BE REPRESENTED AS A NUMBER. THE ENCODER RECEIVES THESE VOLTAGES AND PRESENTS TO THE DIGITAL SECTION THIS NUMBER IN THE FORM OF A SERIES OF 100-KC PULSES. AN ACCURACY OF ONE PART IN $2^{10} = 1024$ IS MAINTAINED. EARTH-CURVATURE CORRECTION IS MADE HERE.
MANUAL SETTING OF PARALLAX CORRECTION
AUX DIGITS INPUTS (12)
DATA PROCESSING SECTION
HERE THE SERIES OF PULSES IS COUNTED AND THE RESULTING NUMBER IS ADDED TO THE ASSOCIATED PARALLAX SETTING AND PRESENTED TO THE OUTPUT SECTION AS A WORD OF BINARY DIGITS, EACH DIGIT OCCUPYING ONE TIME SLOT AND APPEARING AS A "PULSE" OR "LACK-OF-PULSE". AUXILIARY DIGITS ARE ALSO PRESENTED TO THE OUTPUT SECTION AT THE PROPER TIME.
OUTPUT SECTION
THE BINARY WORDS FROM THE DIGITAL SECTION MODULATE THE 1,500-CPS CARRIER. THE SYNCHRONIZING PATTERN ALSO MODULATES THE 1,500-CPS AND 600-CPS CARRIER.
TO TRANSMISSION LINE
CONTROL SIGNALS TO ASSOCIATED EQUIPMENT
CONTROL SIGNALS
1,500-CPS SINE WAVE
REMOTE-START SIGNAL FROM LOCAL RECEIVER
115V AC
POWER SUPPLIES
THE FOLLOWING VOLTAGES ARE REQUIRED:
±300 V DC
+150 V DC
+ 75 V DC
− 20 V DC
+ 4.5 V DC
6.3V AC (FILAMENTS)
PROGRAM GENERATOR
THE PROGRAM GENERATOR SUPPLIES TO EACH CIRCUIT THE PROPER CONTROL SIGNALS AT THE PROPER MOMENTS. THE 1,500-CPS SIGNAL FROM THE OUTPUT SECTION IS USED AS THE MASTER CLOCK. WHEN ARRANGED FOR THE REMOTE START MODE OF OPERATION, A SIGNAL FROM THE LOCAL RECEIVER STARTS THE TRANSMITTER.
CONTROL SIGNALS TO ASSOCIATED EQUIPMENT

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Figure 3. Coordinate data transmitter unit T-721/TSQ-36, functional block diagram.

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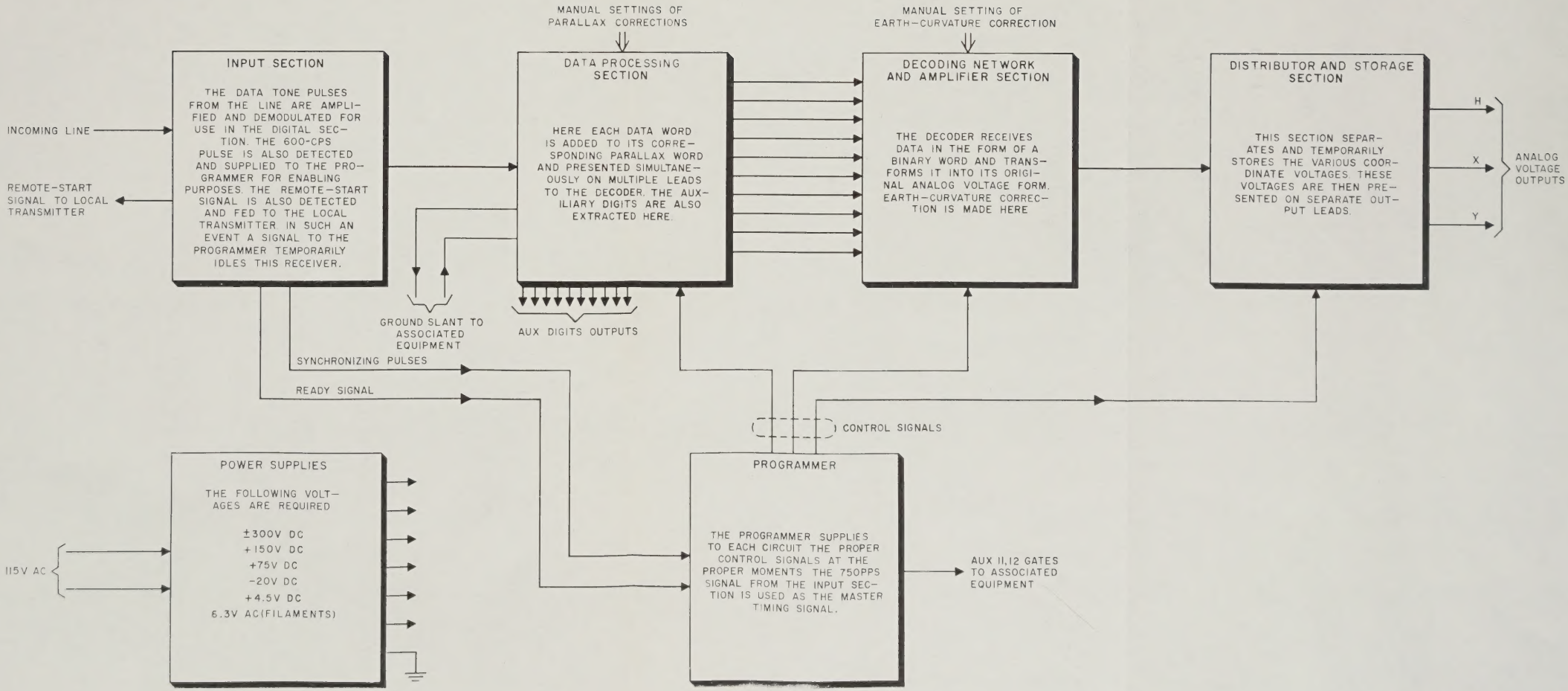
MANUAL SETTINGS OF PARALLAX CORRECTIONS
MANUAL SETTING OF EARTH–CURVATURE CORRECTION
INPUT SECTION
THE DATA TONE PULSES FROM THE LINE ARE AMPLIFIED AND DEMODULATED FOR USE IN THE DIGITAL SECTION. THE 600-CPS PULSE IS ALSO DETECTED AND SUPPLIED TO THE PROGRAMMER FOR ENABLING PURPOSES. THE REMOTE–START SIGNAL IS ALSO DETECTED AND FED TO THE LOCAL TRANSMITTER. IN SUCH AN EVENT A SIGNAL TO THE PROGRAMMER TEMPORARILY IDLES THIS RECEIVER.
DATA PROCESSING SECTION
HERE EACH DATA WORD IS ADDED TO ITS CORRESPONDING PARALLAX WORD AND PRESENTED SIMULTANEOUSLY ON MULTIPLE LEADS TO THE DECODER. THE AUXILIARY DIGITS ARE ALSO EXTRACTED HERE.
DECODING NETWORK AND AMPLIFIER SECTION
THE DECODER RECEIVES DATA IN THE FORM OF A BINARY WORD AND TRANSFORMS IT INTO ITS ORIGINAL ANALOG VOLTAGE FORM. EARTH–CURVATURE CORRECTION IS MADE HERE
DISTRIBUTOR AND STORAGE SECTION
THIS SECTION SEPARATES AND TEMPORARILY STORES THE VARIOUS COORDINATE VOLTAGES. THESE VOLTAGES ARE THEN PRESENTED ON SEPARATE OUTPUT LEADS.
INCOMING LINE
REMOTE–START SIGNAL TO LOCAL TRANSMITTER
H
X
Y
ANALOG VOLTAGE OUTPUTS
GROUND SLANT TO ASSOCIATED EQUIPMENT
AUX DIGITS OUTPUTS
SYNCHRONIZING PULSES
READY SIGNAL
CONTROL SIGNALS
POWER SUPPLIES
THE FOLLOWING VOLTAGES ARE REQUIRED
±300V DC
+150V DC
+75V DC
–20V DC
+4.5V DC
6.3V AC(FILAMENTS)
115V AC
PROGRAMMER
THE PROGRAMMER SUPPLIES TO EACH CIRCUIT THE PROPER CONTROL SIGNALS AT THE PROPER MOMENTS. THE 750PPS SIGNAL FROM THE INPUT SECTION IS USED AS THE MASTER TIMING SIGNAL.
AUX 11,12 GATES TO ASSOCIATED EQUIPMENT

Figure 4. Coordinate data receiver unit R–930/TSQ–36, functional block diagram.

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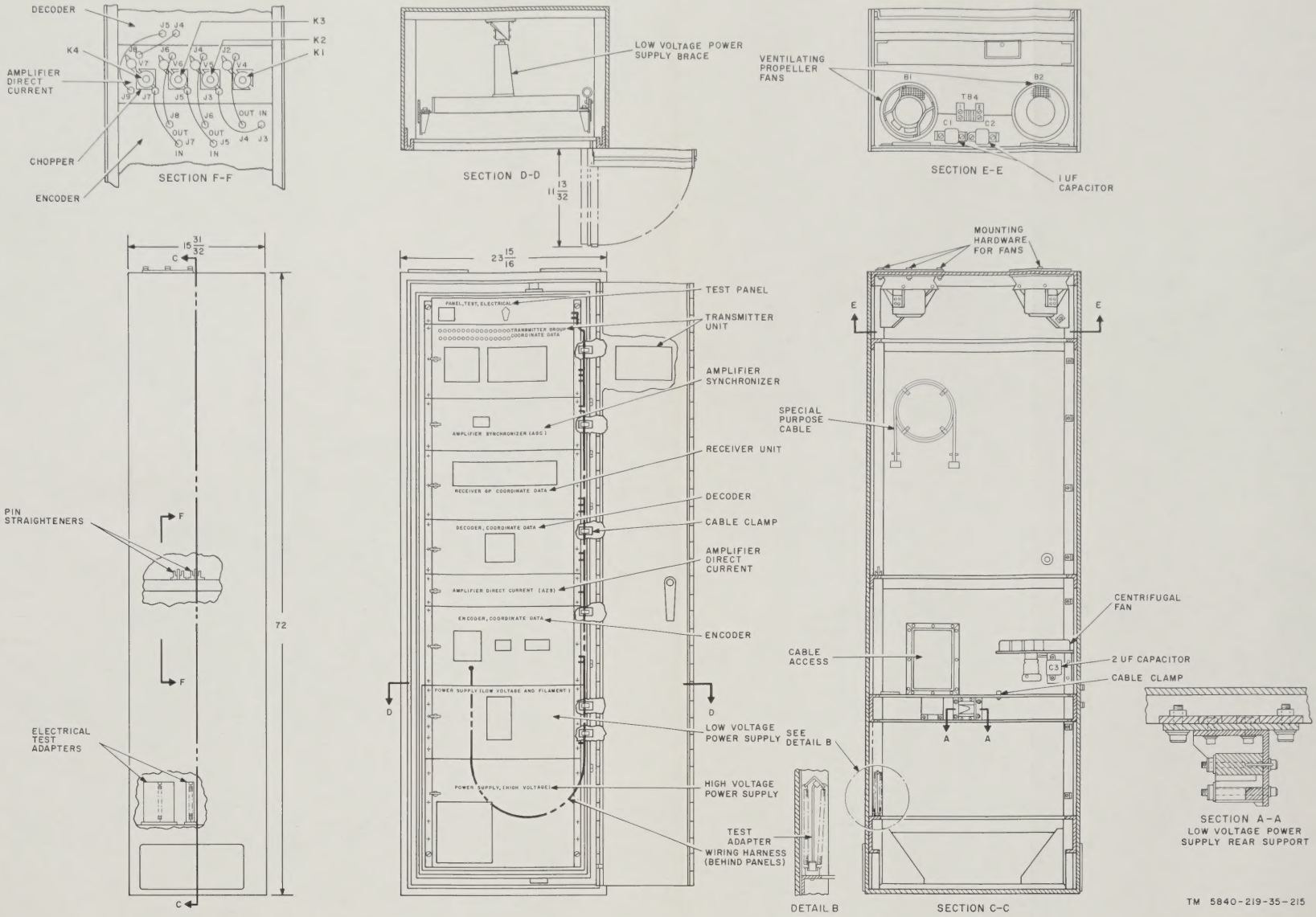

Figure 7. Coordinate data set AN/TSQ-36, installation drawing.

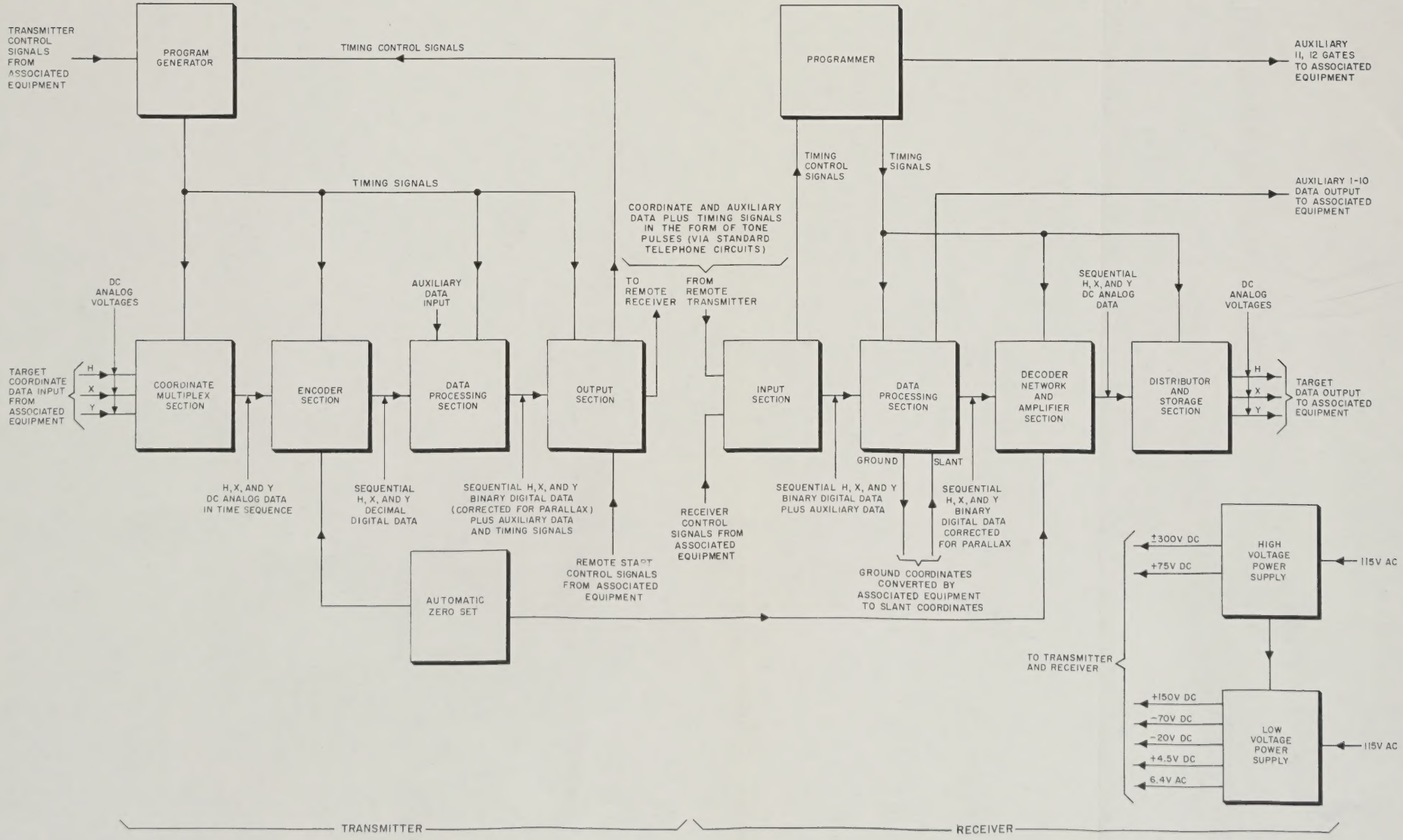
TRANSMITTER CONTROL SIGNALS FROM ASSOCIATED EQUIPMENT
PROGRAM GENERATOR
TIMING CONTROL SIGNALS
PROGRAMMER
AUXILIARY 11, 12 GATES TO ASSOCIATED EQUIPMENT
TIMING SIGNALS
TIMING CONTROL SIGNALS
TIMING SIGNALS
AUXILIARY 1-10 DATA OUTPUT TO ASSOCIATED EQUIPMENT
COORDINATE AND AUXILIARY DATA PLUS TIMING SIGNALS IN THE FORM OF TONE PULSES (VIA STANDARD TELEPHONE CIRCUITS)
DC ANALOG VOLTAGES
AUXILIARY DATA INPUT
TO REMOTE RECEIVER
FROM REMOTE TRANSMITTER
SEQUENTIAL H, X, AND Y DC ANALOG DATA
DC ANALOG VOLTAGES
TARGET COORDINATE DATA INPUT FROM ASSOCIATED EQUIPMENT
H
X
Y
COORDINATE MULTIPLEX SECTION
ENCODER SECTION
DATA PROCESSING SECTION
OUTPUT SECTION
INPUT SECTION
DATA PROCESSING SECTION
DECODER NETWORK AND AMPLIFIER SECTION
DISTRIBUTOR AND STORAGE SECTION
H
X
Y
TARGET DATA OUTPUT TO ASSOCIATED EQUIPMENT
GROUND
SLANT
H, X, AND Y DC ANALOG DATA IN TIME SEQUENCE
SEQUENTIAL H, X, AND Y DECIMAL DIGITAL DATA
SEQUENTIAL H, X, AND Y BINARY DIGITAL DATA (CORRECTED FOR PARALLAX) PLUS AUXILIARY DATA AND TIMING SIGNALS
RECEIVER CONTROL SIGNALS FROM ASSOCIATED EQUIPMENT
SEQUENTIAL H, X, AND Y BINARY DIGITAL DATA PLUS AUXILIARY DATA
SEQUENTIAL H, X, AND Y BINARY DIGITAL DATA CORRECTED FOR PARALLAX
AUTOMATIC ZERO SET
REMOTE START CONTROL SIGNALS FROM ASSOCIATED EQUIPMENT
GROUND COORDINATES CONVERTED BY ASSOCIATED EQUIPMENT TO SLANT COORDINATES
±300V DC
+75V DC
HIGH VOLTAGE POWER SUPPLY
115V AC
TO TRANSMITTER AND RECEIVER
+150V DC
-70V DC
-20V DC
+4.5V DC
6.4V AC
LOW VOLTAGE POWER SUPPLY
115V AC
TRANSMITTER
RECEIVER

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Figure 20. Coordinate data set AN/TSQ-36, basic block diagram.

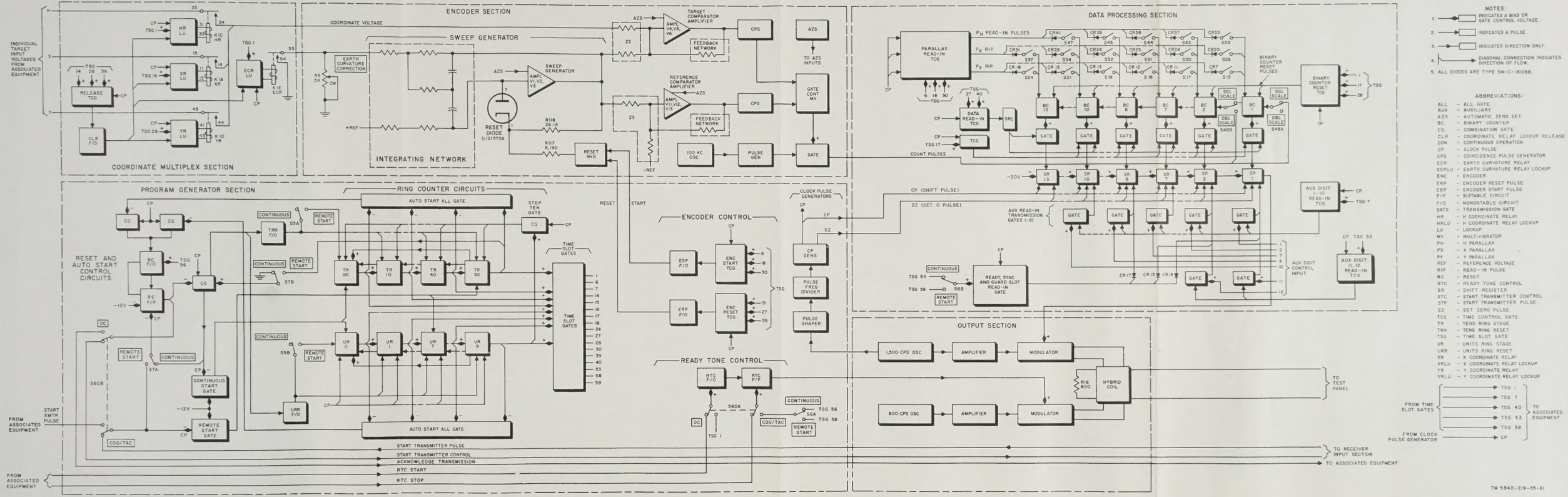

Figure 81. Transmitter, block diagram.

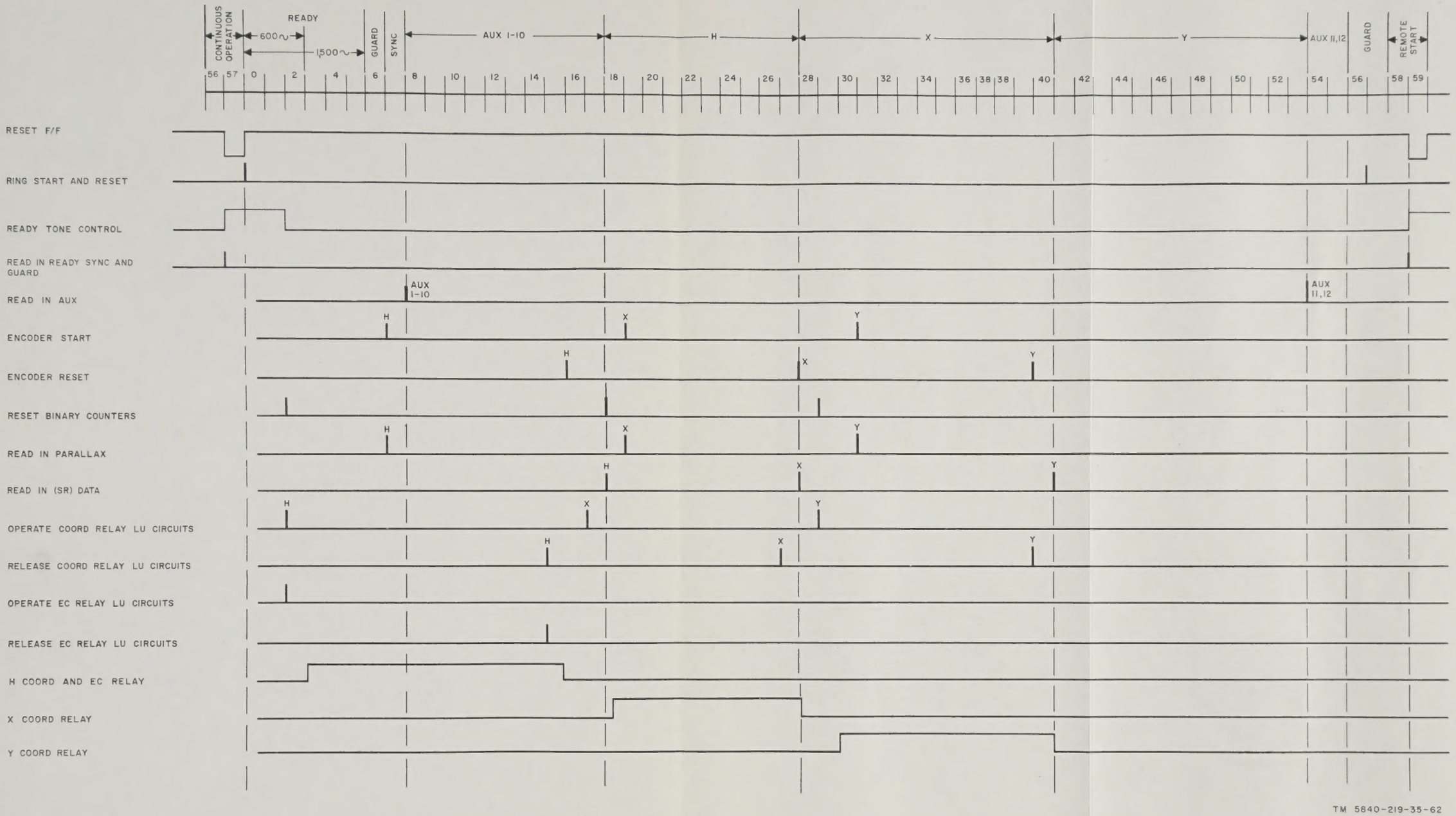

Figure 82. Transmitter, timing diagram.

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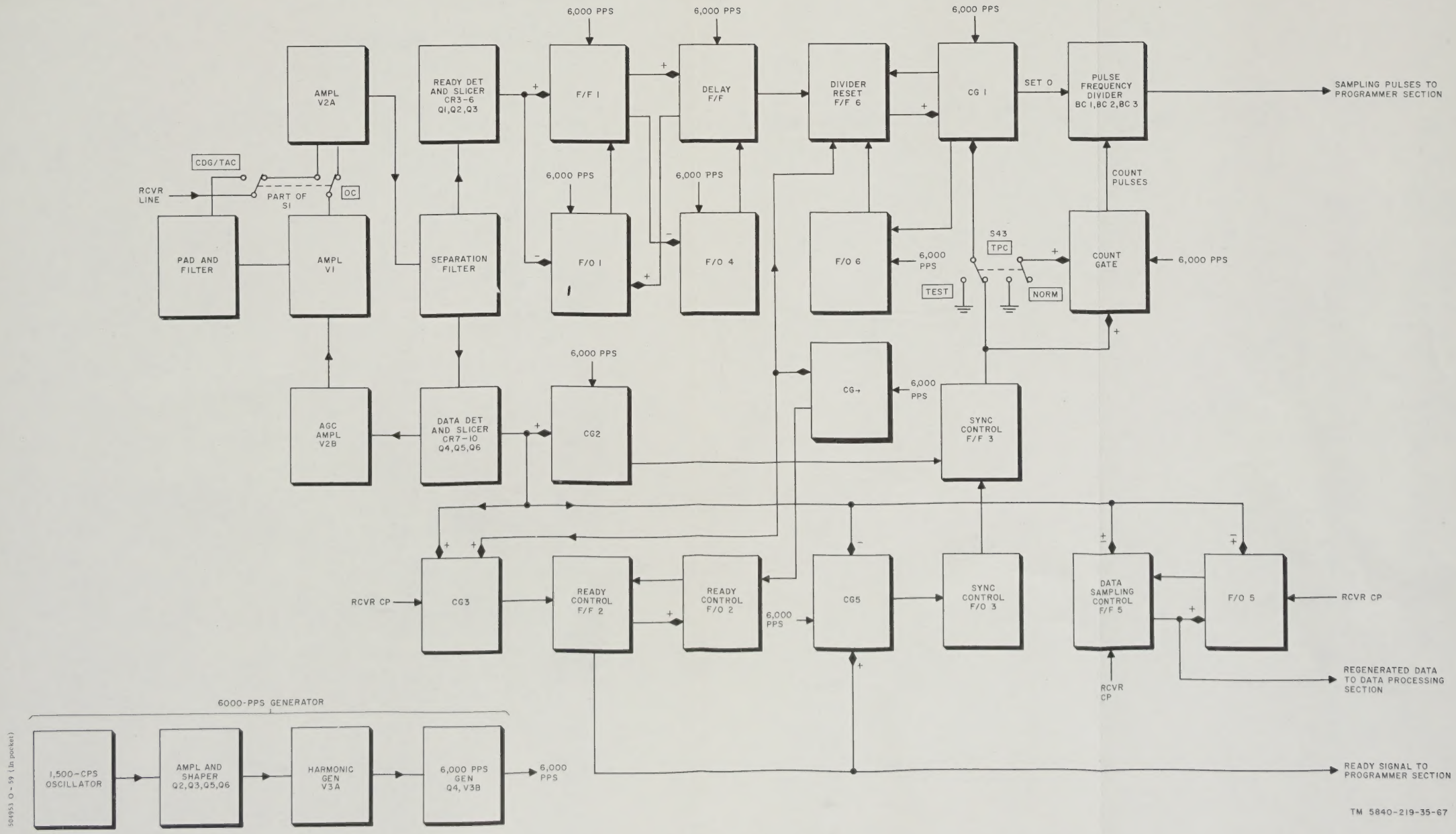
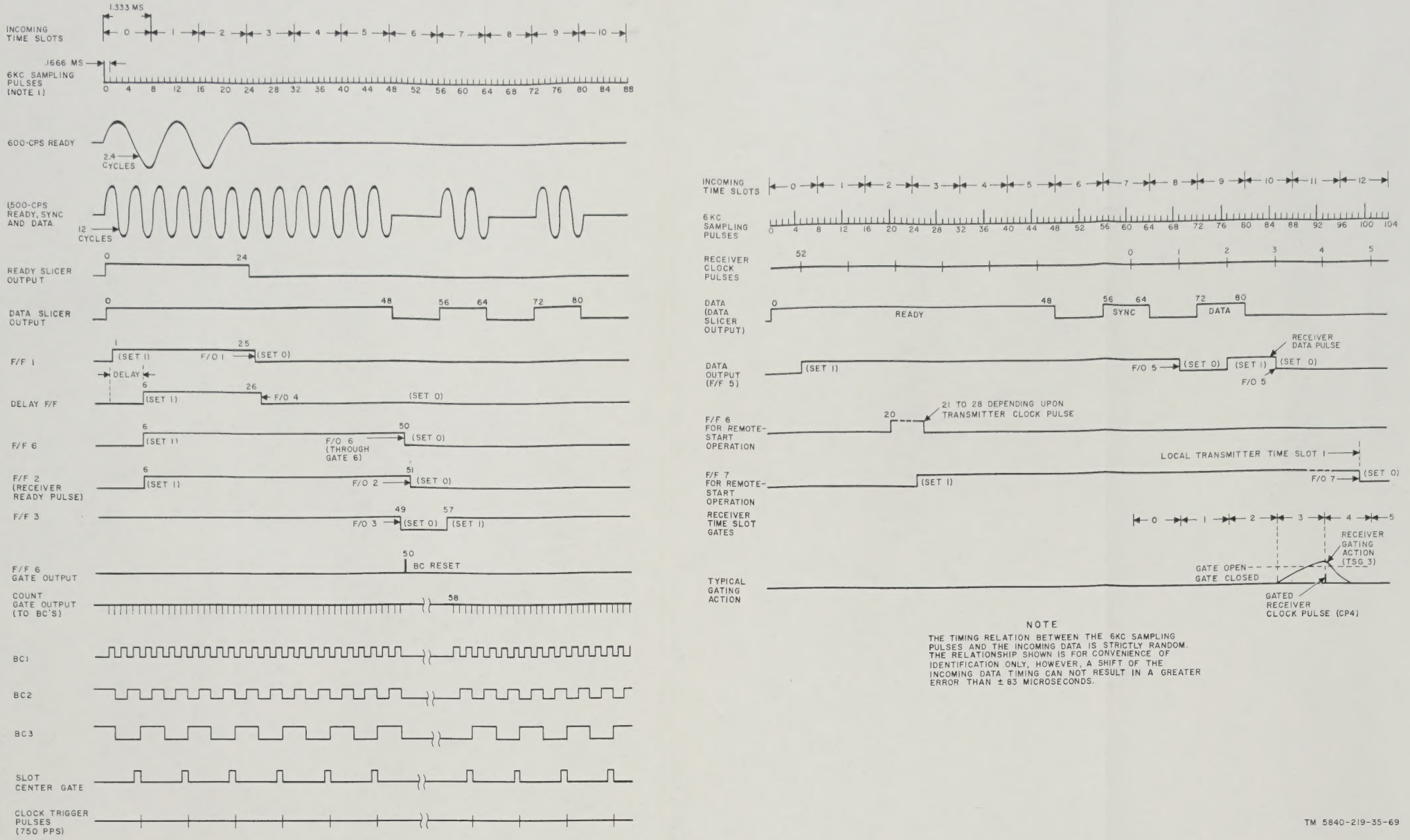


Figure 83. Receiver input section, detailed block diagram.


INCOMING TIME SLOTS
1.333 MS
0 1 2 3 4 5 6 7 8 9 10
.1666 MS
6KC SAMPLING PULSES (NOTE 1)
0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76 80 84 88
600-CPS READY
2.4 CYCLES
1500-CPS READY, SYNC AND DATA
12 CYCLES
READY SLICER OUTPUT
0 24
DATA SLICER OUTPUT
0 48 56 64 72 80
F/F 1
1 (SET 1) 25 F/O 1 (SET 0)
DELAY
DELAY F/F
6 (SET 1) 26 F/O 4 (SET 0)
F/F 6
6 (SET 1) 50 F/O 6 (THROUGH GATE 6) (SET 0)
F/F 2 (RECEIVER READY PULSE)
6 (SET 1) 51 F/O 2 (SET 0)
F/F 3
49 F/O 3 (SET 0) 57 (SET 1)
F/F 6 GATE OUTPUT
50 BC RESET
COUNT GATE OUTPUT (TO BC'S)
58
BC1
BC2
BC3
SLOT CENTER GATE
CLOCK TRIGGER PULSES (750 PPS)
INCOMING TIME SLOTS
0 1 2 3 4 5 6 7 8 9 10 11 12
6KC SAMPLING PULSES
0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76 80 84 88 92 96 100 104
RECEIVER CLOCK PULSES
52 0 1 2 3 4 5
DATA (DATA SLICER OUTPUT)
0 READY 48 56 SYNC 64 72 DATA 80
DATA OUTPUT (F/F 5)
(SET 1) F/O 5 (SET 0) (SET 1) F/O 5 (SET 0)
RECEIVER DATA PULSE
F/F 6 FOR REMOTE-START OPERATION
20 21 TO 28 DEPENDING UPON TRANSMITTER CLOCK PULSE
LOCAL TRANSMITTER TIME SLOT 1
F/F 7 FOR REMOTE-START OPERATION
(SET 1) F/O 7 (SET 0)
RECEIVER TIME SLOT GATES
0 1 2 3 4 5
RECEIVER GATING ACTION (TSG 3)
GATE OPEN
GATE CLOSED
TYPICAL GATING ACTION
GATED RECEIVER CLOCK PULSE (CP4)

NOTE

THE TIMING RELATION BETWEEN THE 6KC SAMPLING PULSES AND THE INCOMING DATA IS STRICTLY RANDOM. THE RELATIONSHIP SHOWN IS FOR CONVENIENCE OF IDENTIFICATION ONLY, HOWEVER, A SHIFT OF THE INCOMING DATA TIMING CAN NOT RESULT IN A GREATER ERROR THAN ± 83 MICROSECONDS.

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Figure 88. Receiver input section, timing diagram.

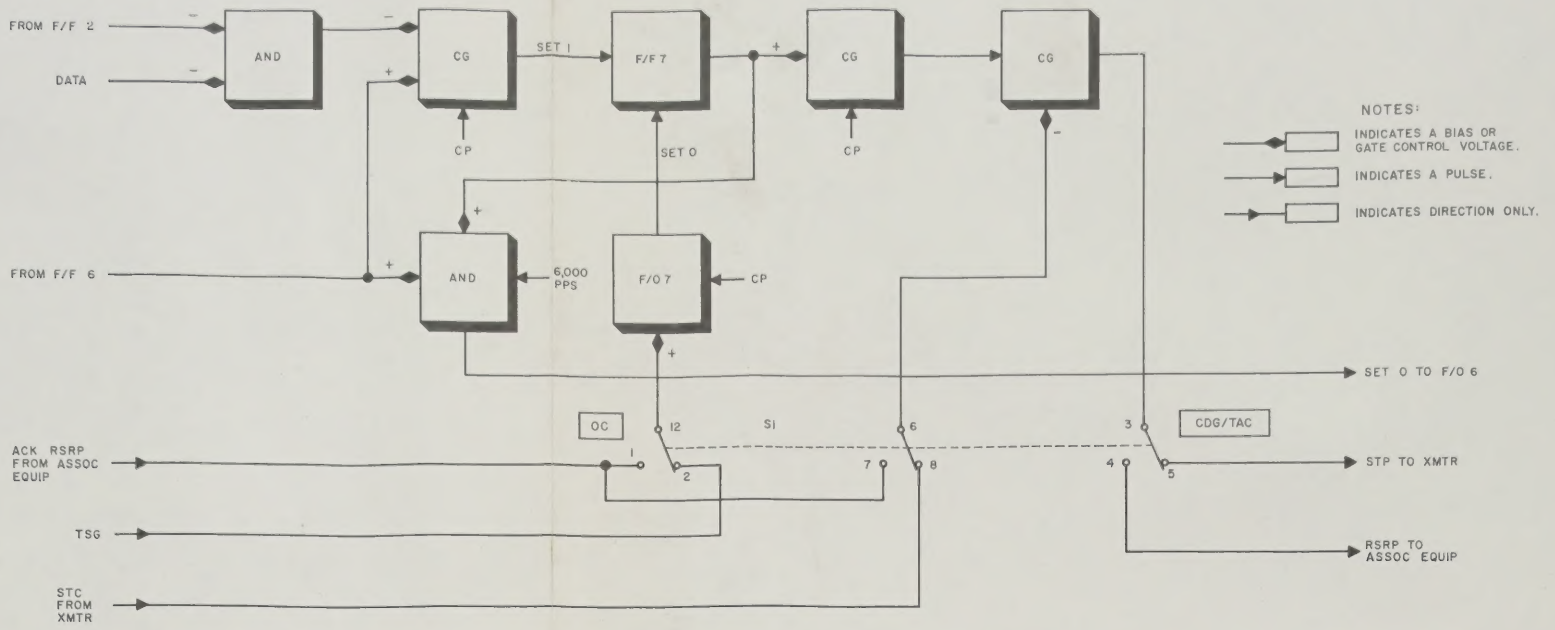

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Figure 101.—Remote start circuits, block diagram.

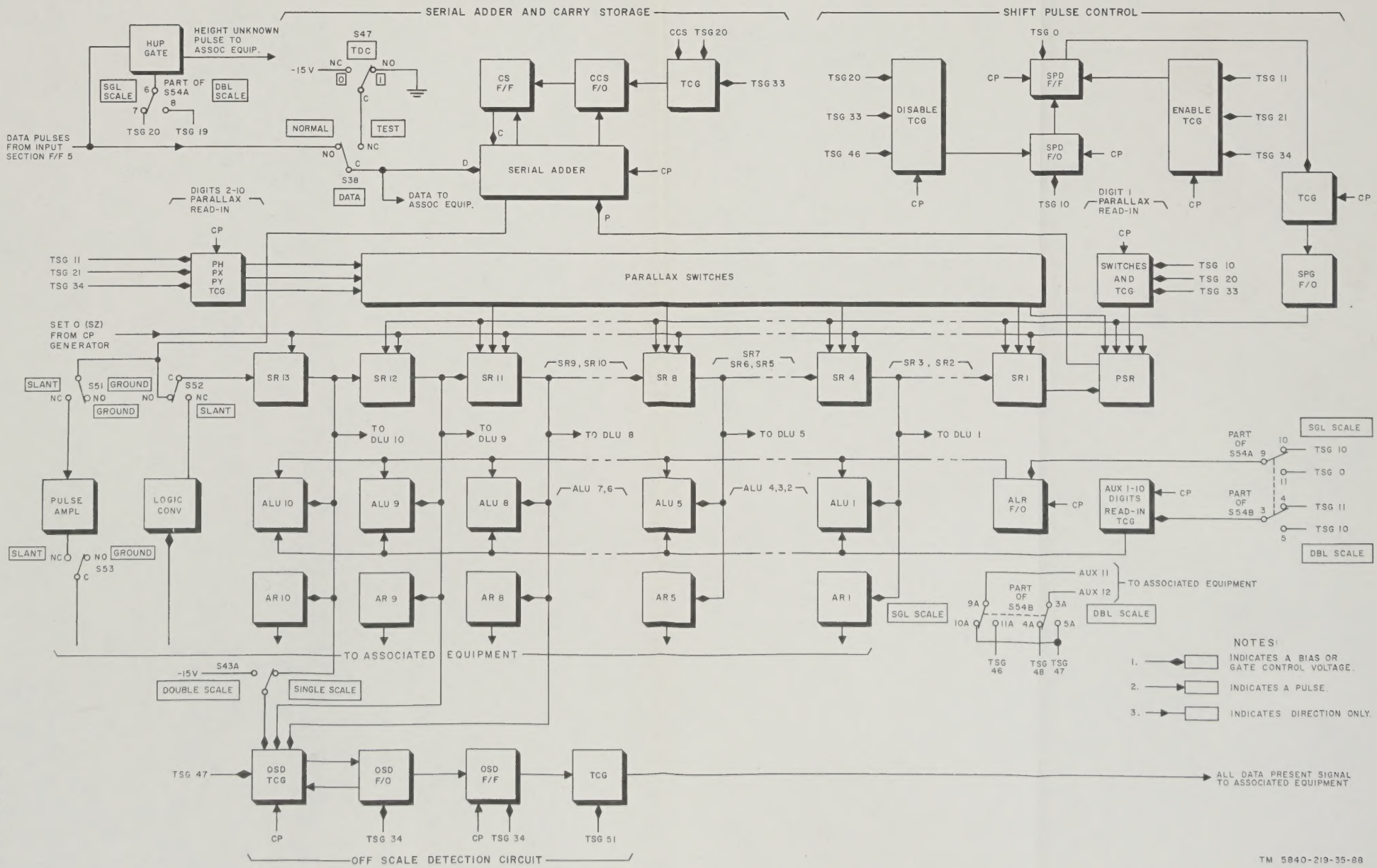

Figure 108. Receiver data processing, block diagram.

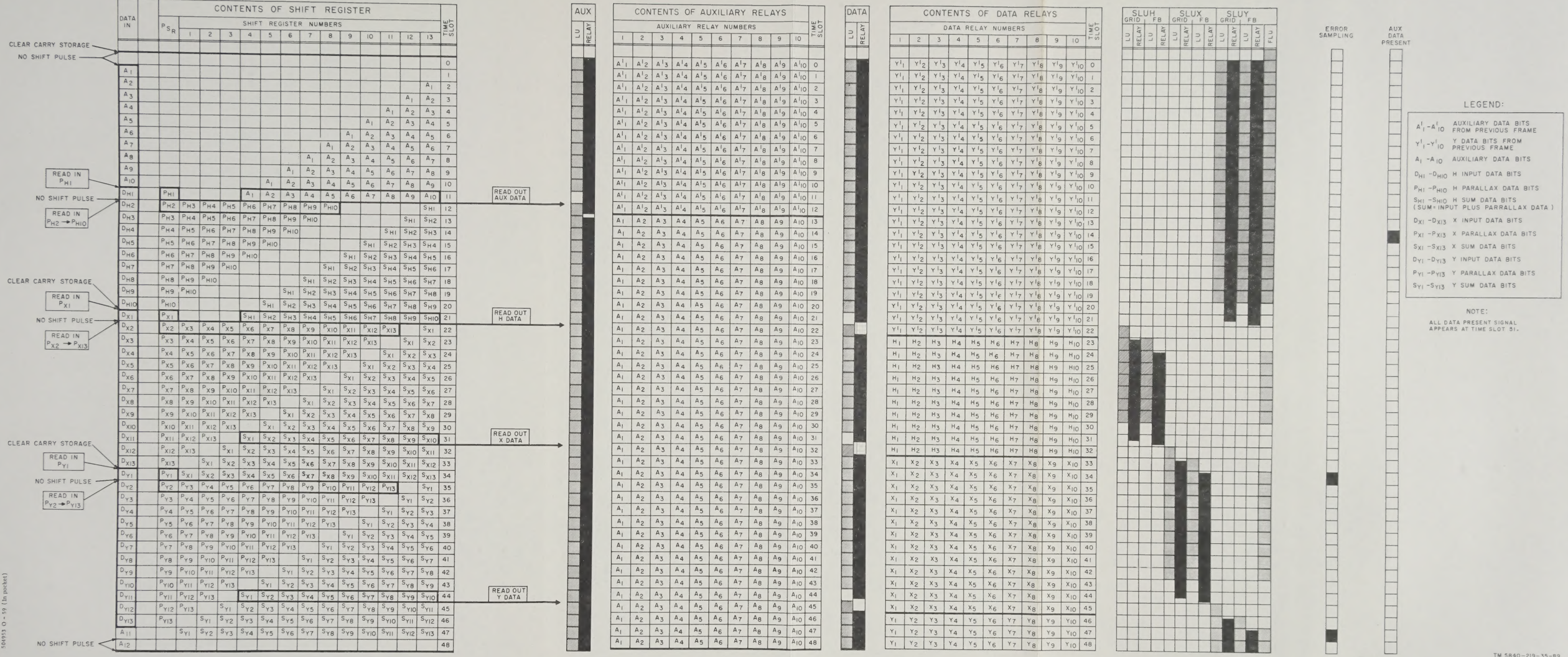

Figure 109. Receiver data processing section, general timing diagrams.

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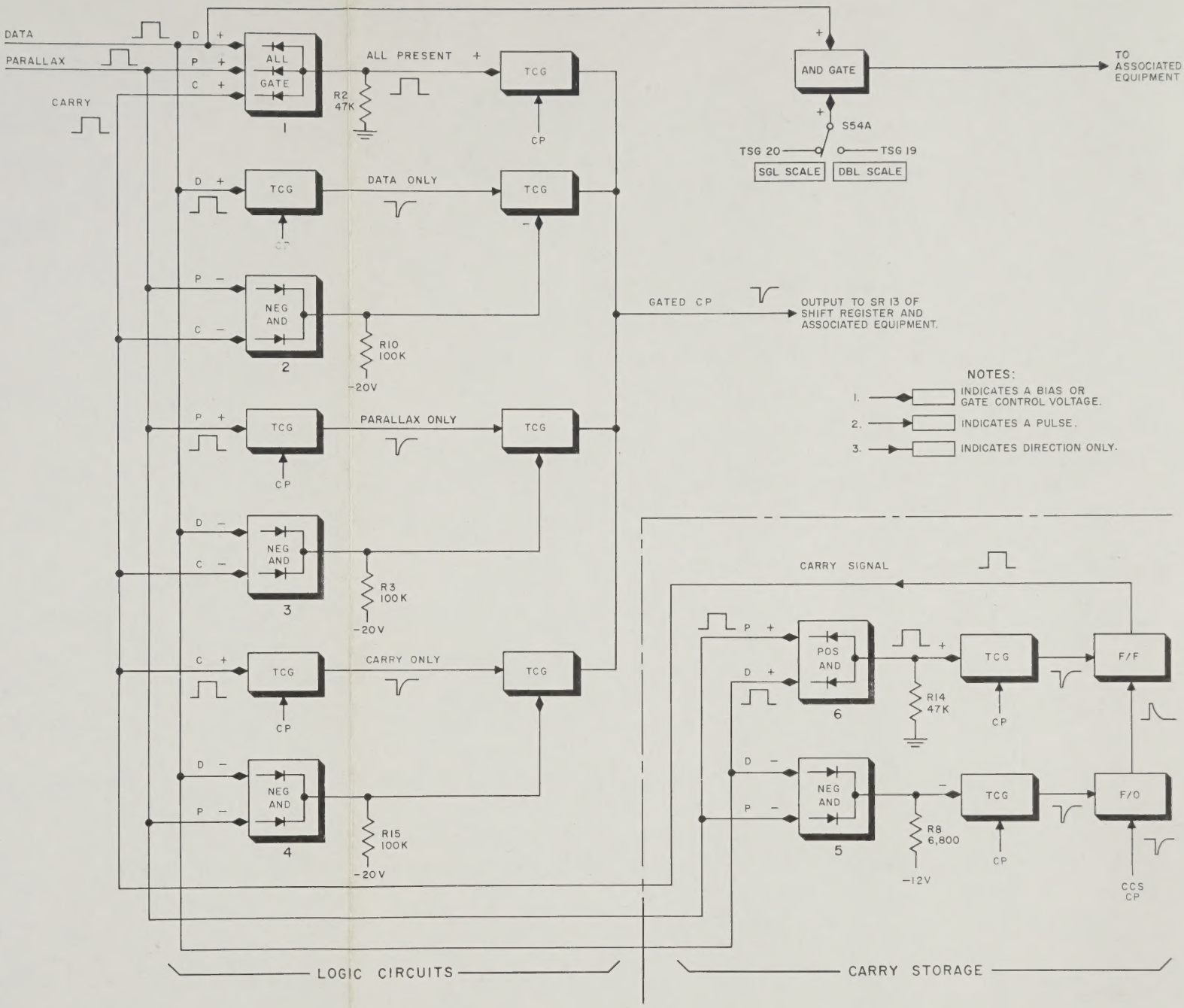

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Figure 111. Serial adder, block diagram.

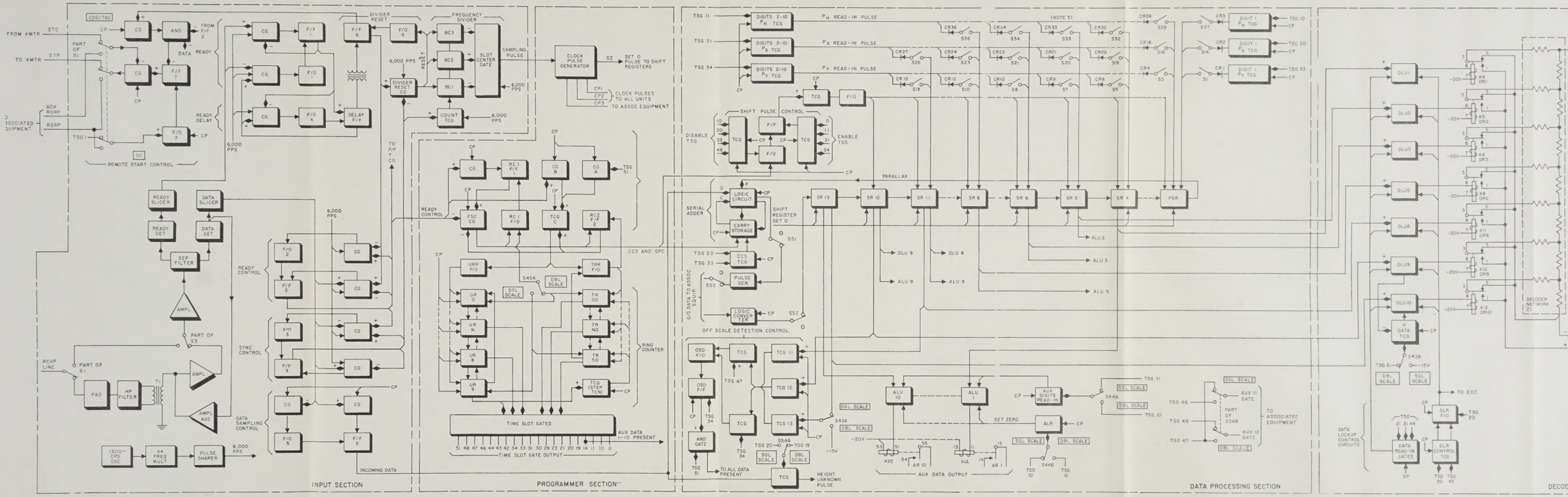

Figure 131. Receiver, block diagram.

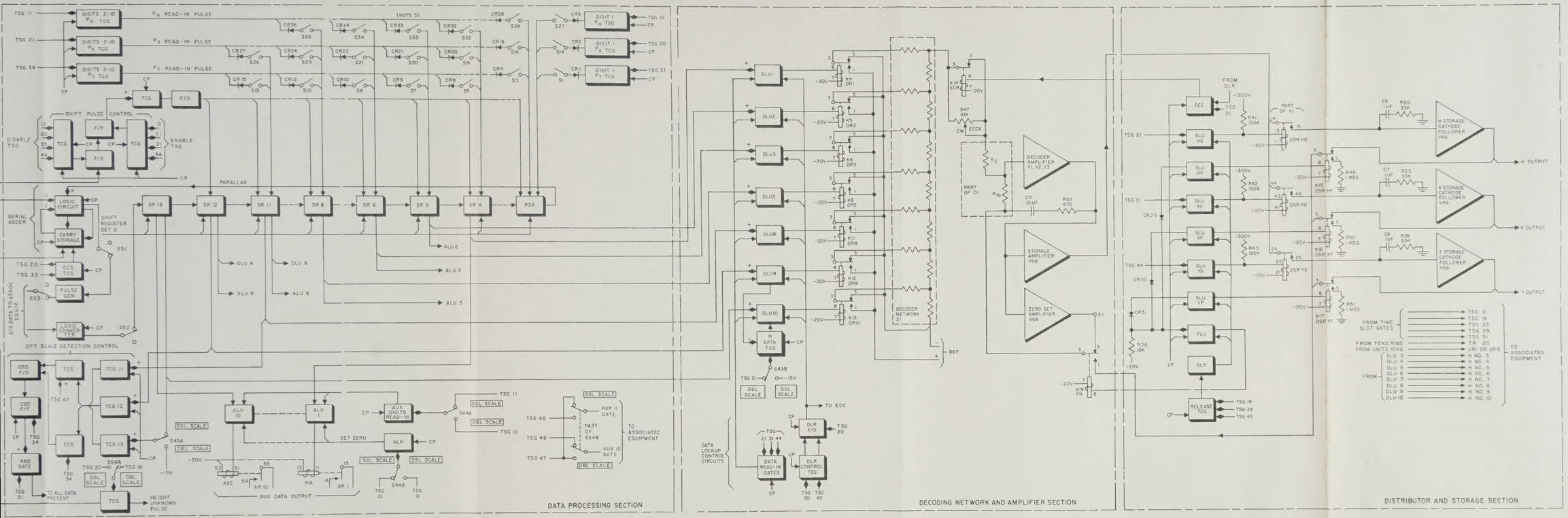
DATA PROCESSING SECTION
DECODING NETWORK AND AMPLIFIER SECTION
DISTRIBUTOR AND STORAGE SECTION
OFF SCALE DETECTION CONTROL
SHIFT PULSE CONTROL
PARALLAX
SERIAL ADDER
DISABLE TSG
ENABLE TSG
AUX DATA OUTPUT
DATA LOCKUP CONTROL CIRCUITS
DECODER NETWORK Z1
TO ASSOCIATED EQUIPMENT
H OUTPUT
X OUTPUT
Y OUTPUT
ABBREVIATIONS:
ADC - ALL DATA CONTROL LEAD
AGC - AUTOMATIC GAIN CONTROL
ALU - AUXILIARY (AUX) LOCKUP
ALR - AUX LOCKUP RELEASE
AR - AUX RELAY
BC - BINARY COUNTER
CCS - CLEAR CARRY STORAGE
CG - COMBINATION GATE
CP - CLOCK PULSE
DLU - DATA LOCKUP
DLR - DATA LOCKUP RELEASE
DR - DATA RELAY
DSA - DATA STORAGE AMPLIFIER
DSR - DATA STORAGE RELAY
ECC - EARTH CURVATURE CORRECTION
ECCA - EARTH CURVATURE CORRECTION ADJUST
ECCLU - EARTH CURVATURE CORRECTION LOCKUP
ECR - EARTH CURVATURE RELAY
F/F - BISTABLE CIRCUIT
F/O - MONOSTABLE CIRCUIT
FSC - FRAME START CONTROL
FLU - FEEDBACK LOCKUP
FR - FEEDBACK RELAY
HF - H COORDINATE FEEDBACK
HG - H COORDINATE GRID
PSR - PARALLAX STORAGE REGISTER
RFB - FEEDBACK RESISTANCE
RLU - REFERENCE LOCKUP
RPD - REFERENCE PROTECTION DELAY
RPLU - REFERENCE SHORT CIRCUIT PROTECTION LOCKUP
RPR - REFERENCE SHORT CIRCUIT RELAY
RS - REMOTE START
RS - SERIES RESISTANCE
SLU - STORAGE LOCKUP
SLR - STORAGE LOCKUP RELEASE
SP - SAMPLING PULSE
SPC - SHIFT PULSE CONTROL
SR - SHIFT REGISTER
TCG - TIME CONTROL GATE
TR - TENS RING
TRR - TENS RING RESET
TSG - TIME SLOT GATE
UR - UNITS RING
URR - UNITS RING RESET
XF - X COORDINATE FEEDBACK
XG - X COORDINATE GRID
YF - Y COORDINATE FEEDBACK
YG - Y COORDINATE GRID
NOTES:
1. INDICATES A BIAS OR GATE CONTROL VOLTAGE
2. INDICATES A PULSE.
3. INDICATES DIRECTION ONLY
4. DIAGONAL CONNECTION INDICATES DIRECTION OF FLOW.
5. ALL TIME SLOT GATE VOLTAGES ARE POSITIVE.
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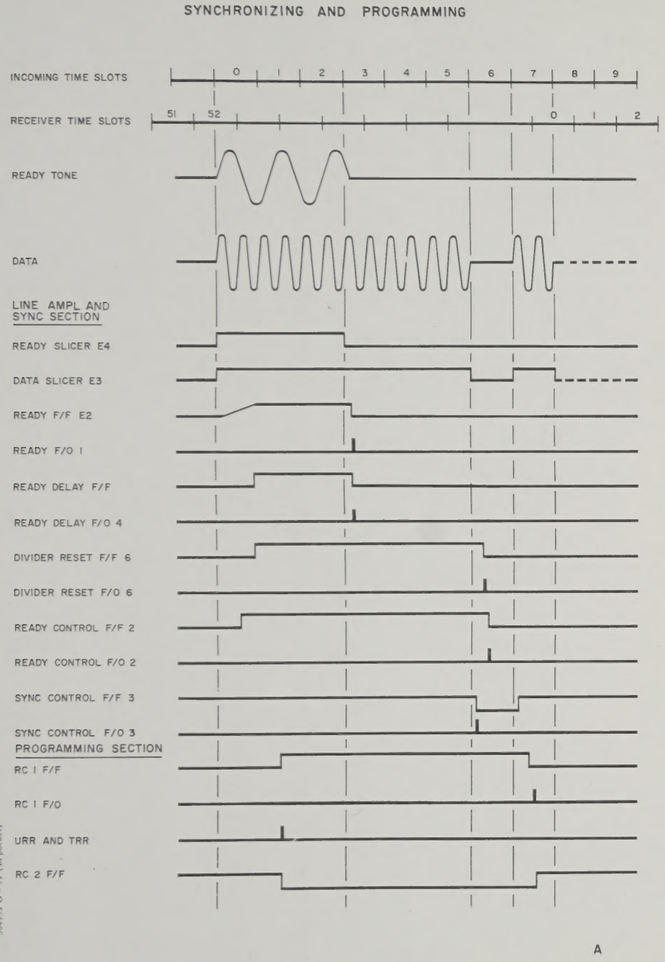
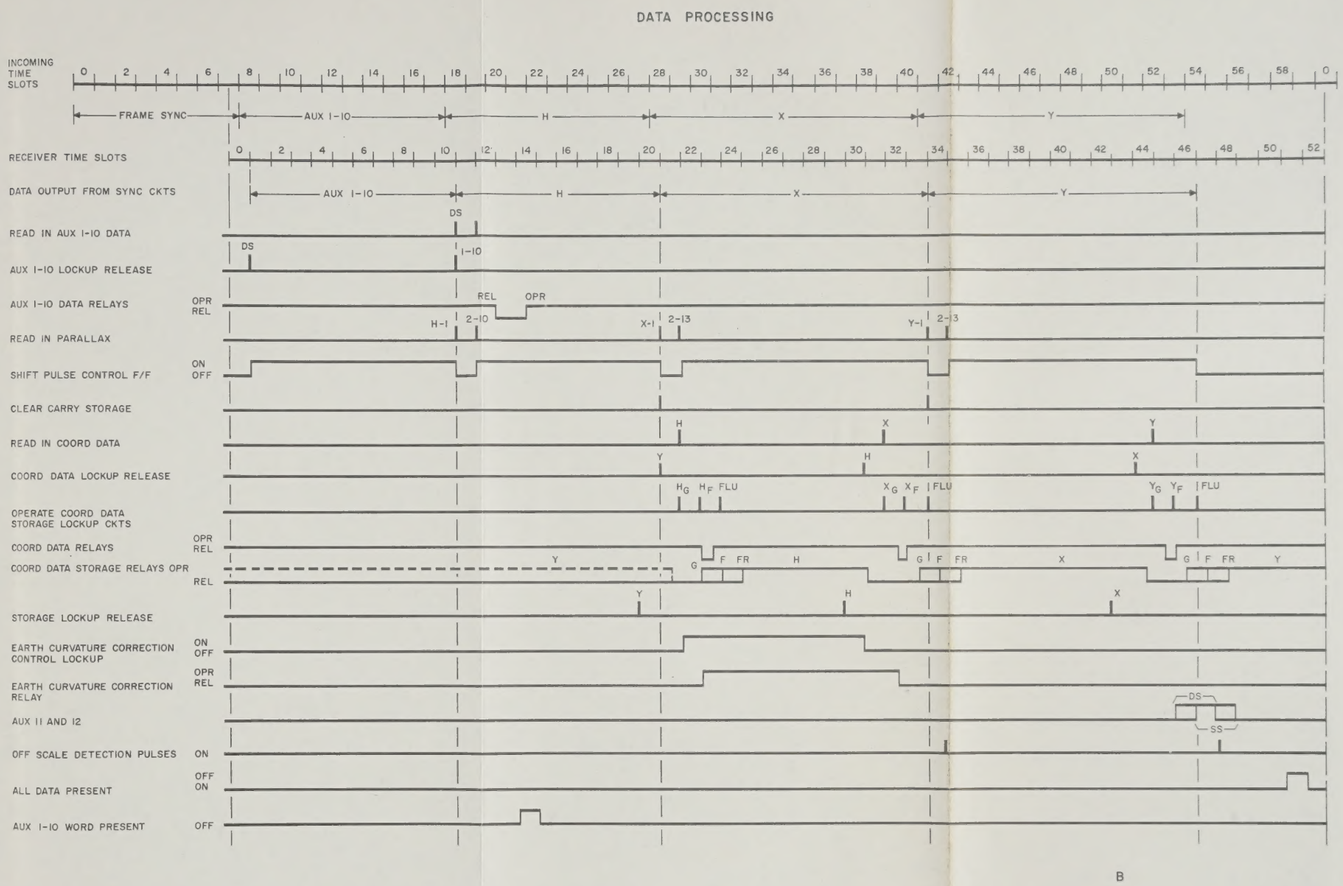
Figure 131. Receiver, block diagram.



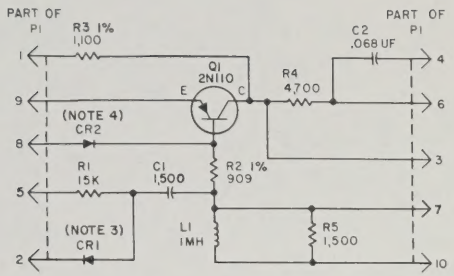


ABBREVIATION	FUNCTIONAL DESIGNATION
AUX	AUXILIARY
DS	DOUBLE SCALE
F	FEEDBACK RELAY
F/F	BISTABLE CIRCUIT
FLU	FEEDBACK LOCKUP
F/O	MONOSTABLE CIRCUIT
FR	FEEDBACK RELAY
G	GRID RELAY
H	H COORDINATE
H_F	H COORDINATE FEEDBACK
H_G	H COORDINATE GRID
SS	SINGLE SCALE
TRR	TENS RING RESET
URR	UNITS RING RESET
X	X COORDINATE
X_F	X COORDINATE FEEDBACK
X_G	X COORDINATE GRID
Y	Y COORDINATE
Y_F	Y COORDINATE FEEDBACK
Y_G	Y COORDINATE GRID

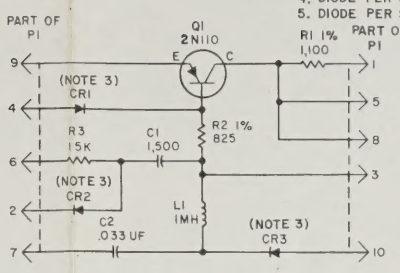
Figure 132. Receiver, timing diagram.

NOTES:

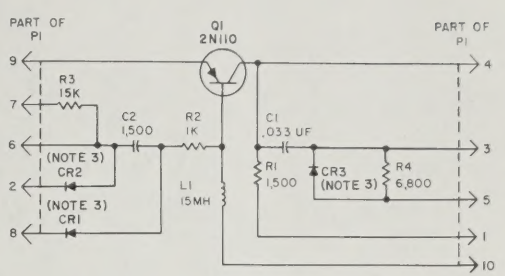
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED. RESISTORS ARE ± 5% TOLERANCE.
3. DIODE PER SM-B-181088.
4. DIODE PER SM-B-181094.
5. DIODE PER SM-B-181092.



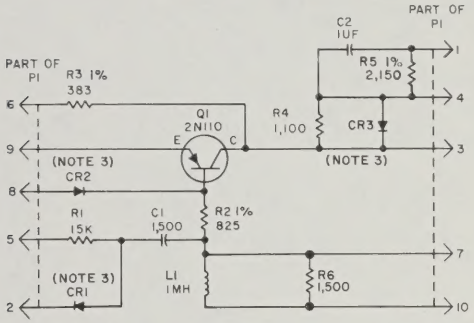
A PACKAGE



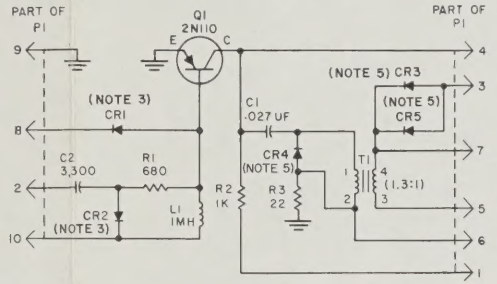
B PACKAGE



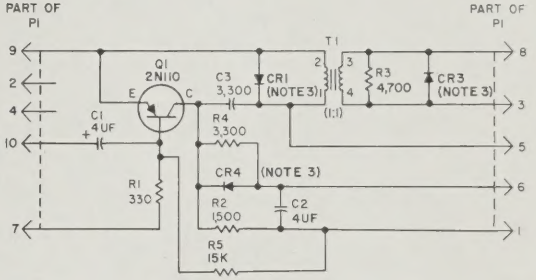
C PACKAGE



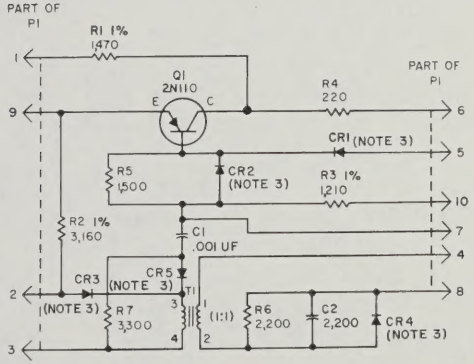
D PACKAGE



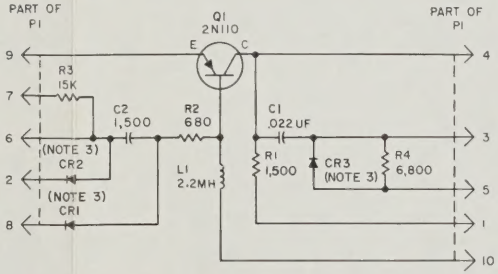
E PACKAGE



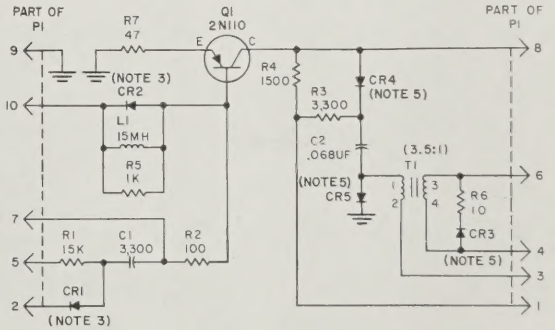
J PACKAGE



K PACKAGE



L PACKAGE



M PACKAGE

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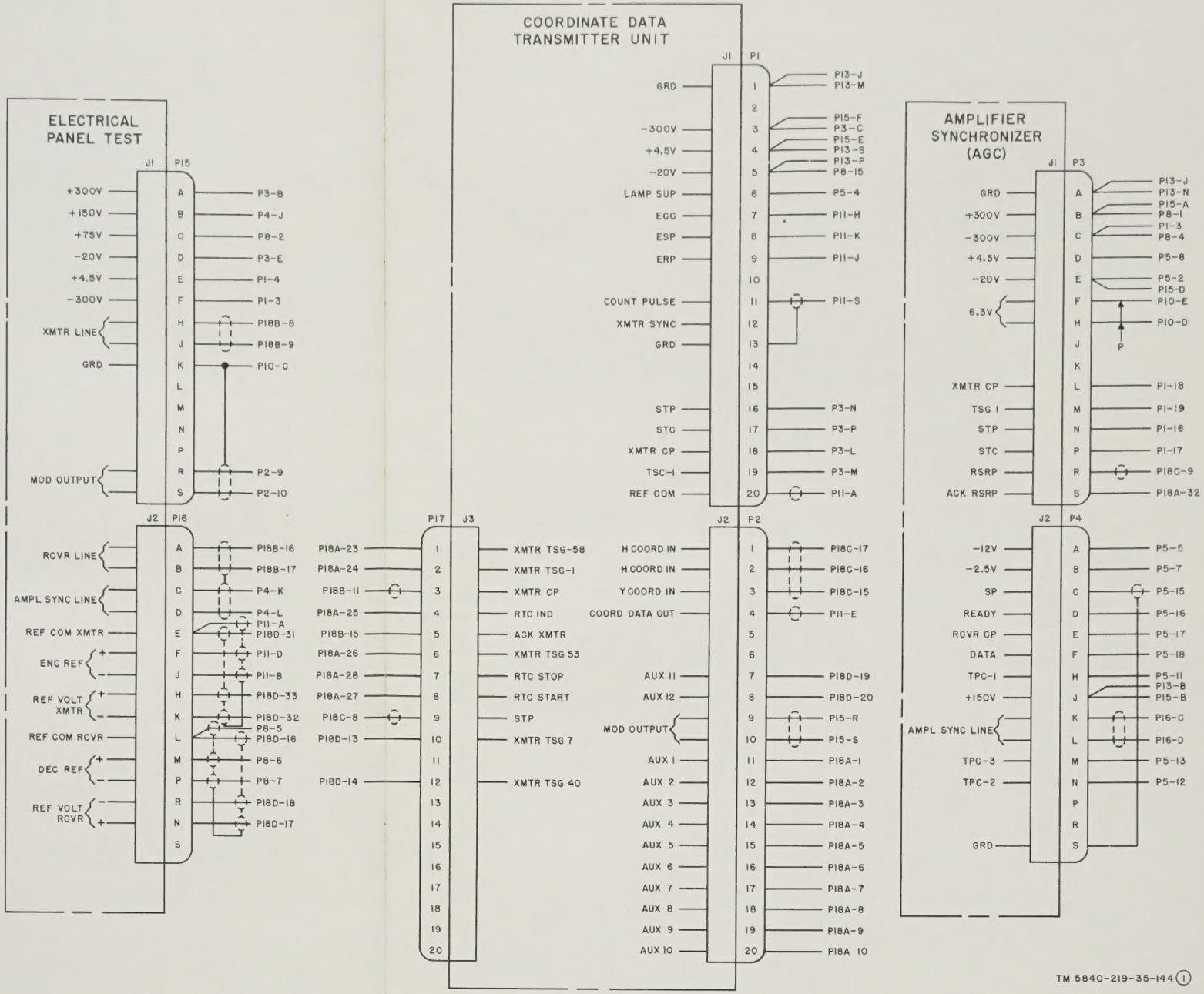
Figure 133. Package schematics.

504953 O - 59 (In pocket)



504953 O - 59 (In pocket)

TM 5840-219-35-144 (1)

Figure 162. Coordinate data set AN/TSQ-36, interconnecting schematic.

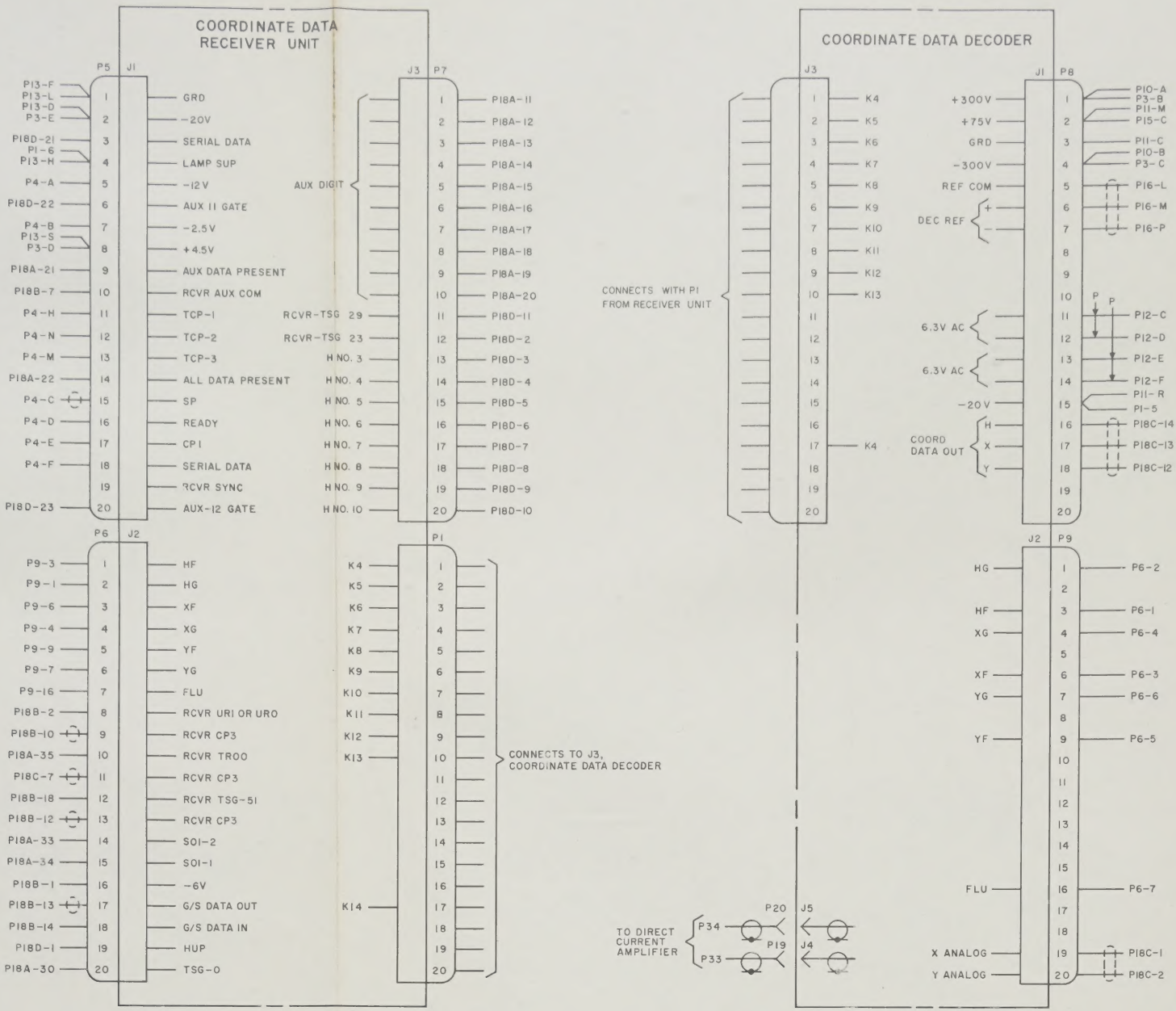


Figure 162—Continued.

TM 5840-219-35-144 (2)

504953 O - 59 (In pocket)

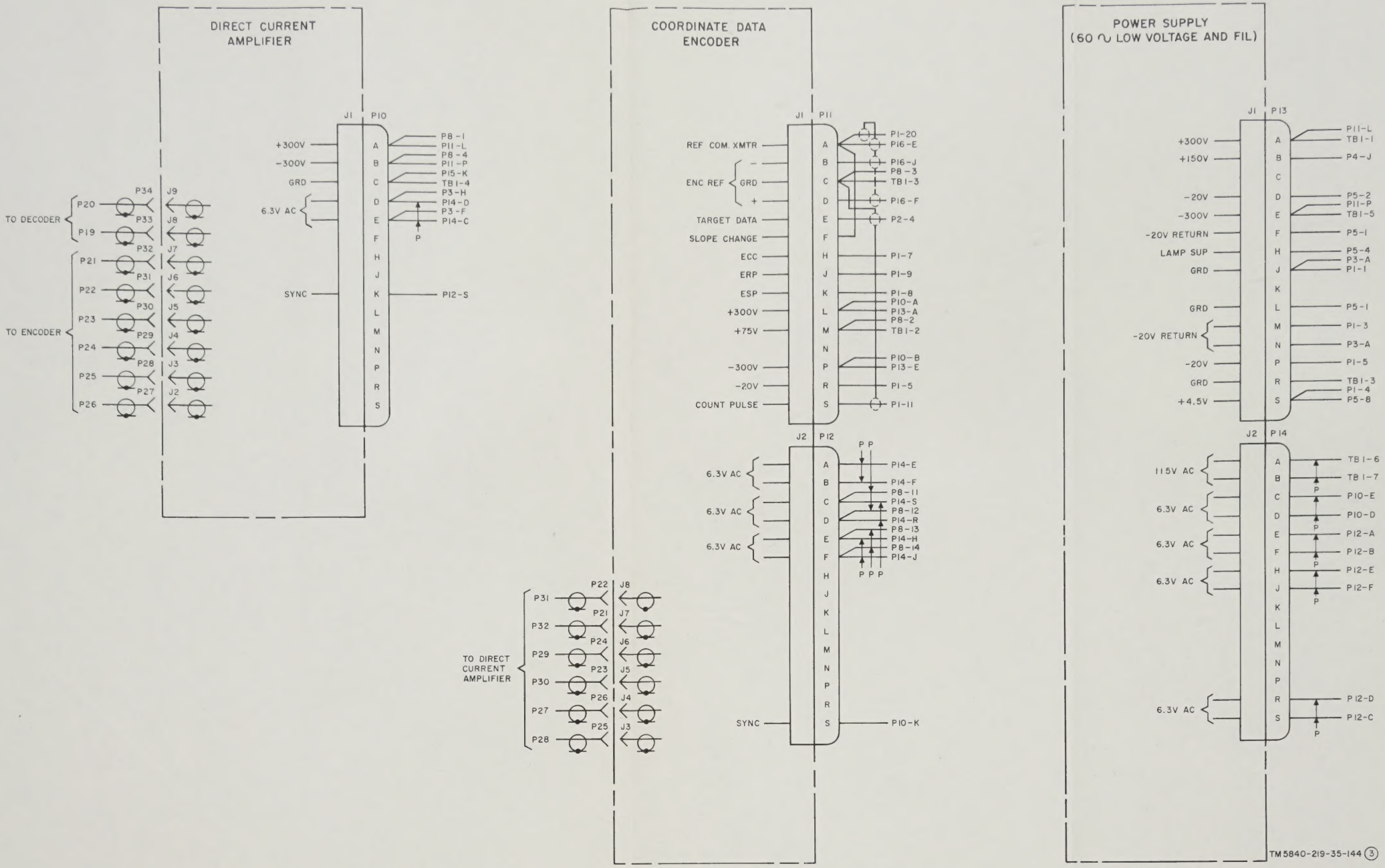


Figure 162—Continued.

504953 O - 59 (In pocket)

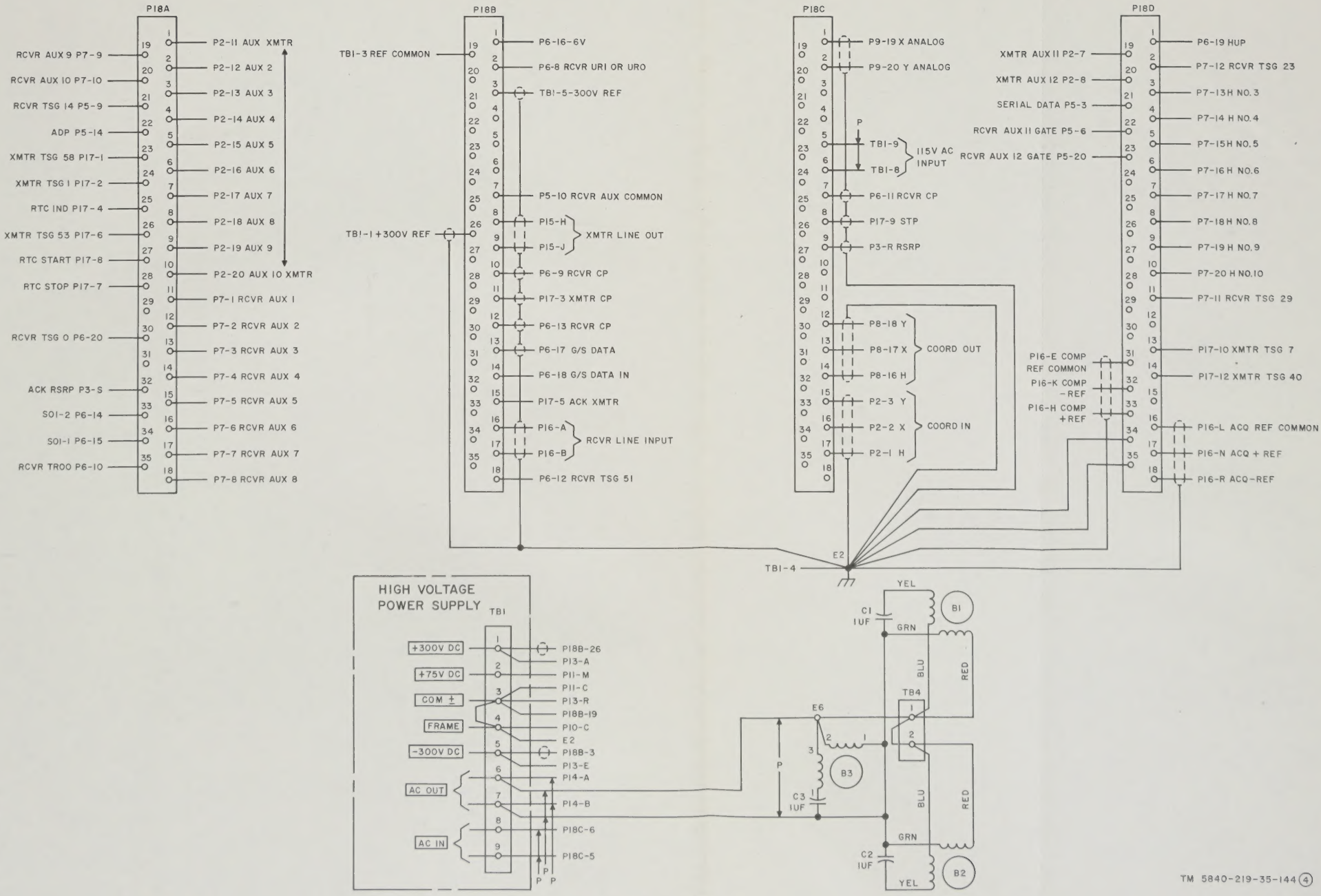


Figure 162—Continued.

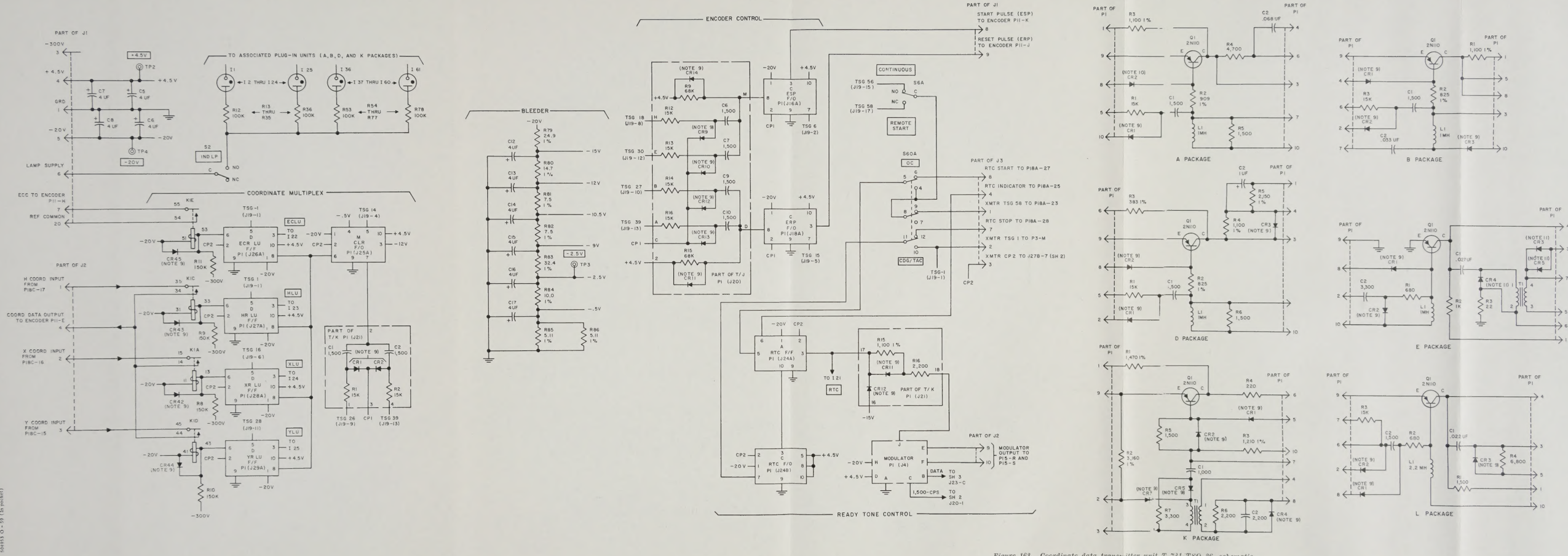
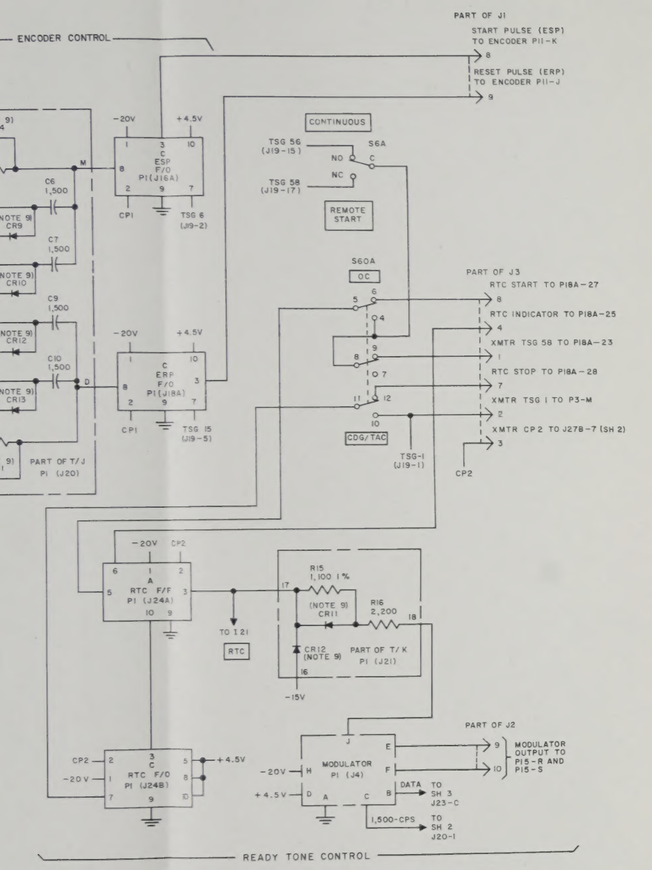
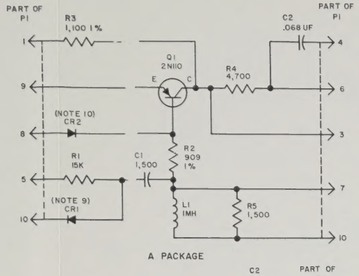
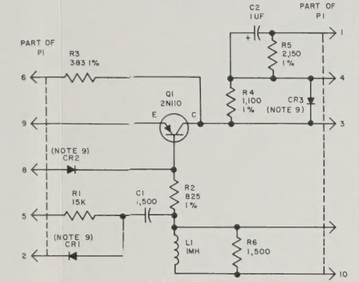
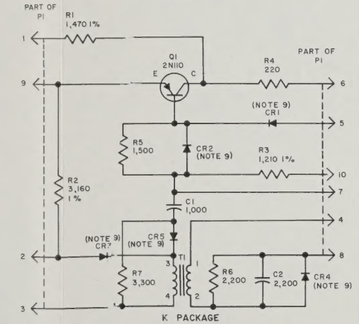


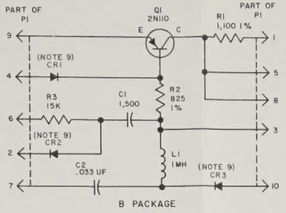
Figure 163. Coordinate data transmitter unit T-721/TSQ-36, schematic.

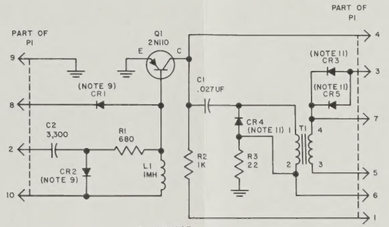


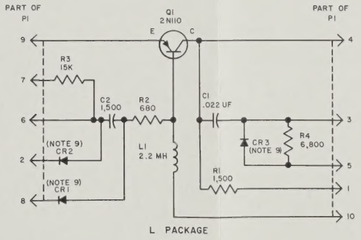


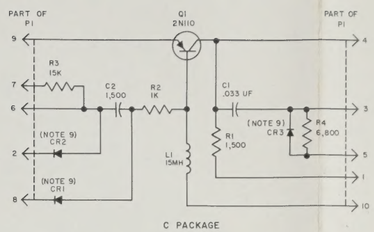


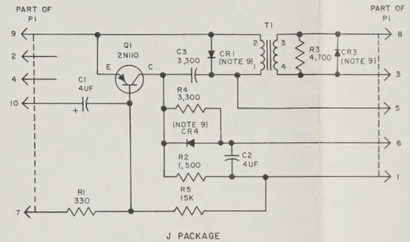












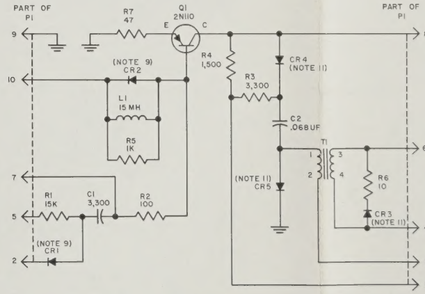
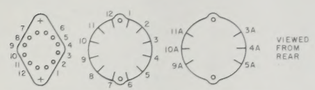


Figure 163. Coordinate data transmitter unit T-721/TSQ-36, schematic.

NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±5% TOLERANCE.
3. TERMINAL NUMBERING FOR SWITCHES S10, S11, S60A, AND S60B IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM BELOW.



4. ENCLOSURES DESIGNATED A, B, T/J, T/K ETC REPRESENT PLUG-IN UNITS. THE J NUMBER ASSOCIATED WITH P1 IN THE ENCLOSURES IS THE DESIGNATION OF THE MATING PANEL CONNECTOR. THE NUMBERS ASSOCIATED WITH LEADS ENTERING THE ENCLOSURE ARE THE PLUG AND CONNECTOR TERMINALS.
5. NONFUNCTIONAL PLUG-IN UNITS MAY APPEAR IN SEVERAL ENCLOSURES FOR CIRCUIT LAYOUT CONVENIENCE. TERMINALS ARE REPEATED IN THESE ENCLOSURES WHERE NECESSARY TO FACILITATE CIRCUIT READABILITY.
6. THE FUNCTIONAL DESIGNATIONS ASSOCIATED WITH THE LAMP CONNECTIONS AT THE UNIT RING, TENS RING, BINARY COUNTER, AND SHIFT REGISTER STAGES INDICATE STAGE NUMBERS OF THE UNITS RING, TENS RING, BINARY COUNTER, AND SHIFT REGISTER RESPECTIVELY.
7. FUNCTIONAL PACKAGE DESIGNATIONS ARE EXPLAINED IN TABLE A.
8. ☐ INDICATES EQUIPMENT MARKING.
9. DIODE PER SM-B-181088.
10. DIODE PER SM-B-181094.
11. DIODE PER SM-B-181092.
12. TRANSISTOR PER SM-B-182553.

TABLE A

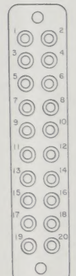
ABBREVIATION	FUNCTIONAL DESIGNATION
ACK	ACKNOWLEDGE
BC 1-13	BINARY COUNTERS
CLR	COORDINATE RELAY LOCKUP RELEASE
CO	CONTINUOUS
CP1 AND 2	CLOCK PULSE GENERATOR
ECR	EARTH CURVATURE CORRECTION RELAY
ERP	ENCODER RESET PULSE
ESP	ENCODER START PULSE
HR	H COORDINATE RELAY
PC	PULSE CONTROL
PFD	PULSE FREQUENCY DIVIDER
PH	H COORDINATE PARALLAX
PX	X COORDINATE PARALLAX
PY	Y COORDINATE PARALLAX
RS	REMOTE START
RT	PROGRAMMER RESET CONTROL
RTC	READY TONE CONTROL
SP	SINGLE PULSE GENERATOR
SR 1-13	SHIFT REGISTER
SRC	SHIFT REGISTER CONTROL
SZ	SHIFT REGISTER SET ZERO PULSE
TC	RECYCLE TEST CONTROL
TR 00-50	TENS RING
TRR	TENS RING RESET PULSE GENERATOR
UR 0-9	UNITS RING
URR	UNITS RING RESET PULSE GENERATOR
XR	X COORDINATE RELAY
YR	Y COORDINATE RELAY
LU	LOCKUP
F/F	BISTABLE CIRCUIT (FLIP-FLOP)
F/O	MONOSTABLE CIRCUIT (FLIP-ZERO)

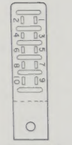
HIGHEST REFERENCE DESIGNATIONS

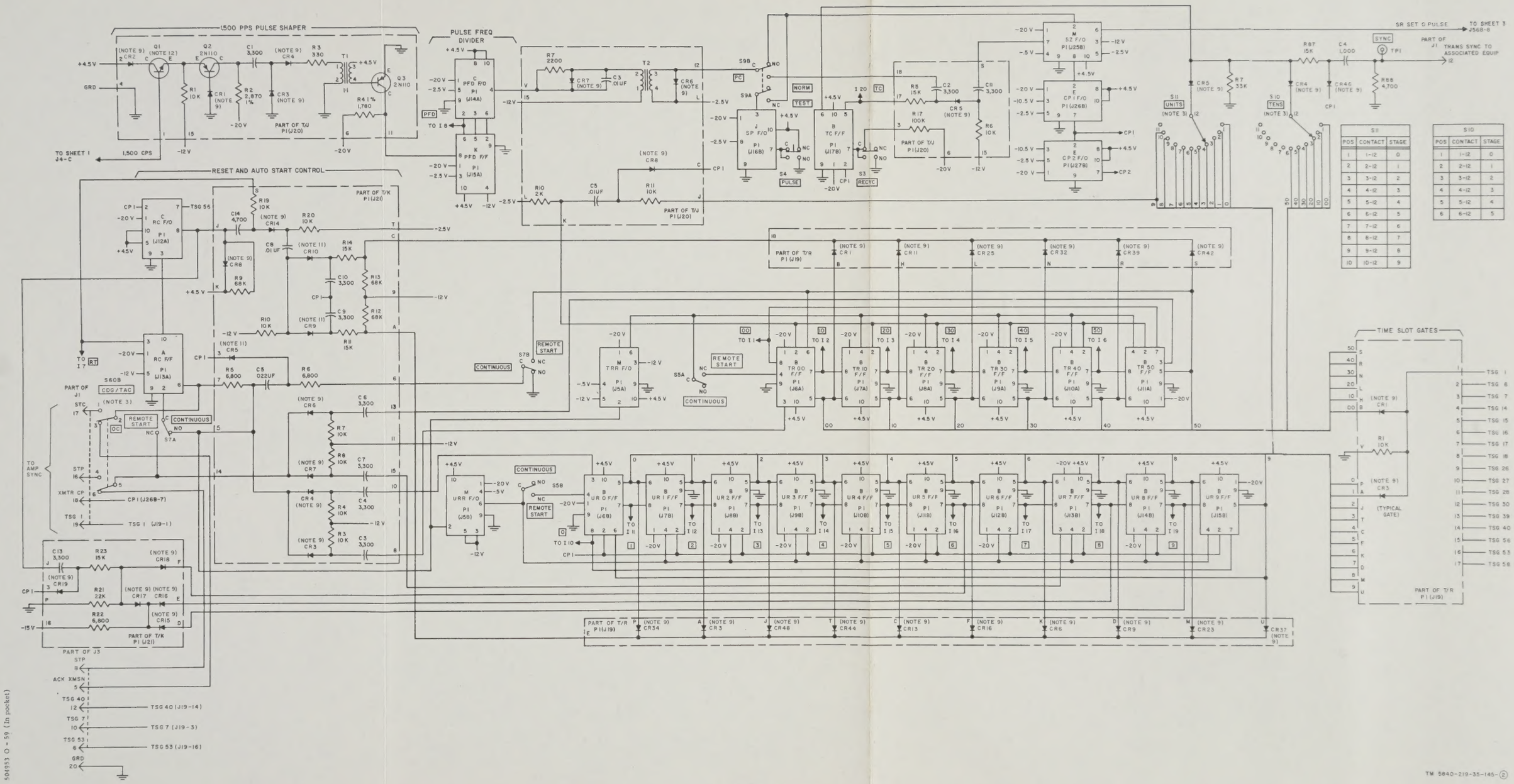
C17 CR46 R89

REFERENCE DESIGNATIONS NOT USED

C9, C10, C11, R20 R37 THRU R52 INCL







S11		
POS	CONTACT	STAGE
1	1-12	0
2	2-12	1
3	3-12	2
4	4-12	3
5	5-12	4
6	6-12	5
7	7-12	6
8	8-12	7
9	9-12	8
10	10-12	9

S10		
POS	CONTACT	STAGE
1	1-12	0
2	2-12	1
3	3-12	2
4	4-12	3
5	5-12	4
6	6-12	5

Figure 163—Continued.

504953 O - 59 (In pocket)

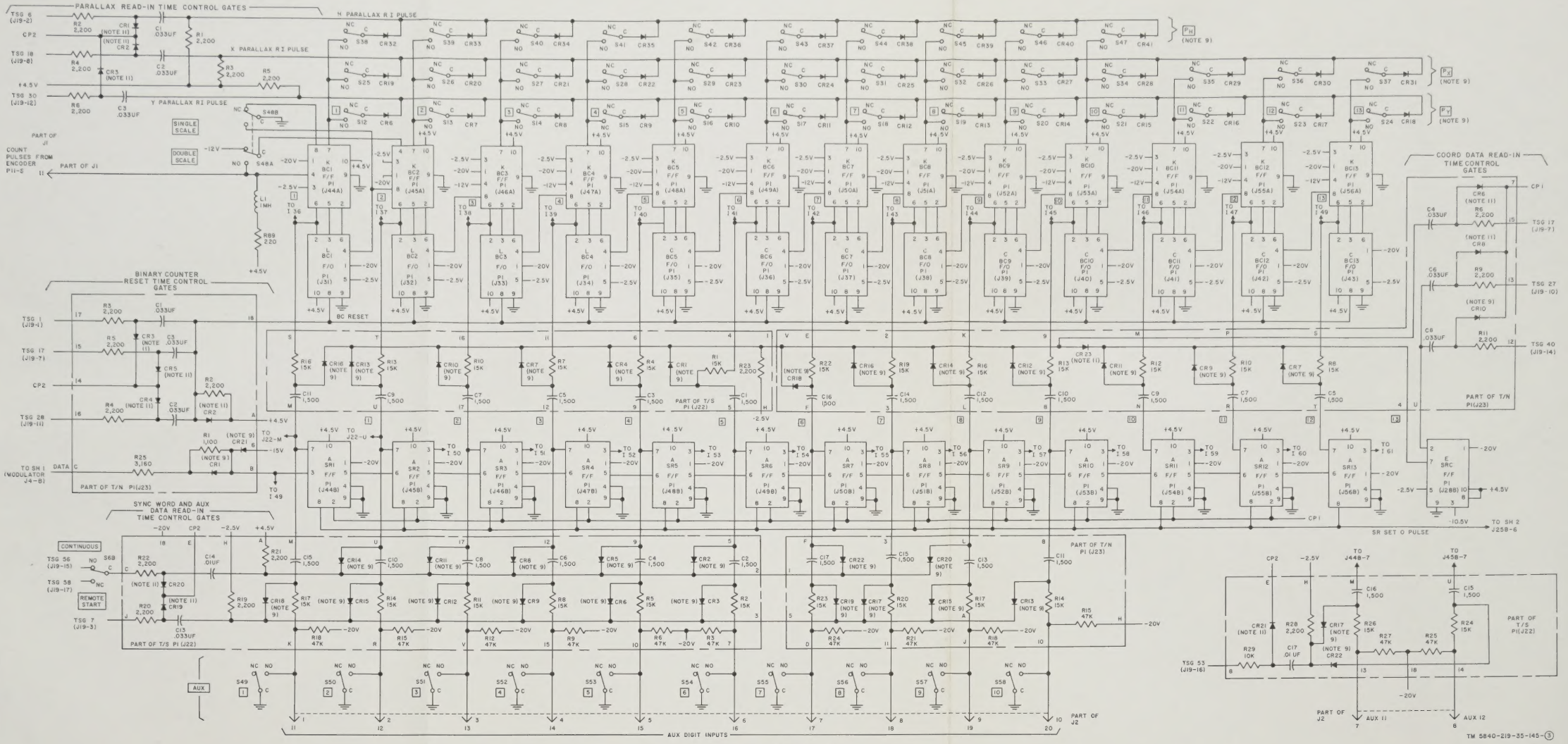
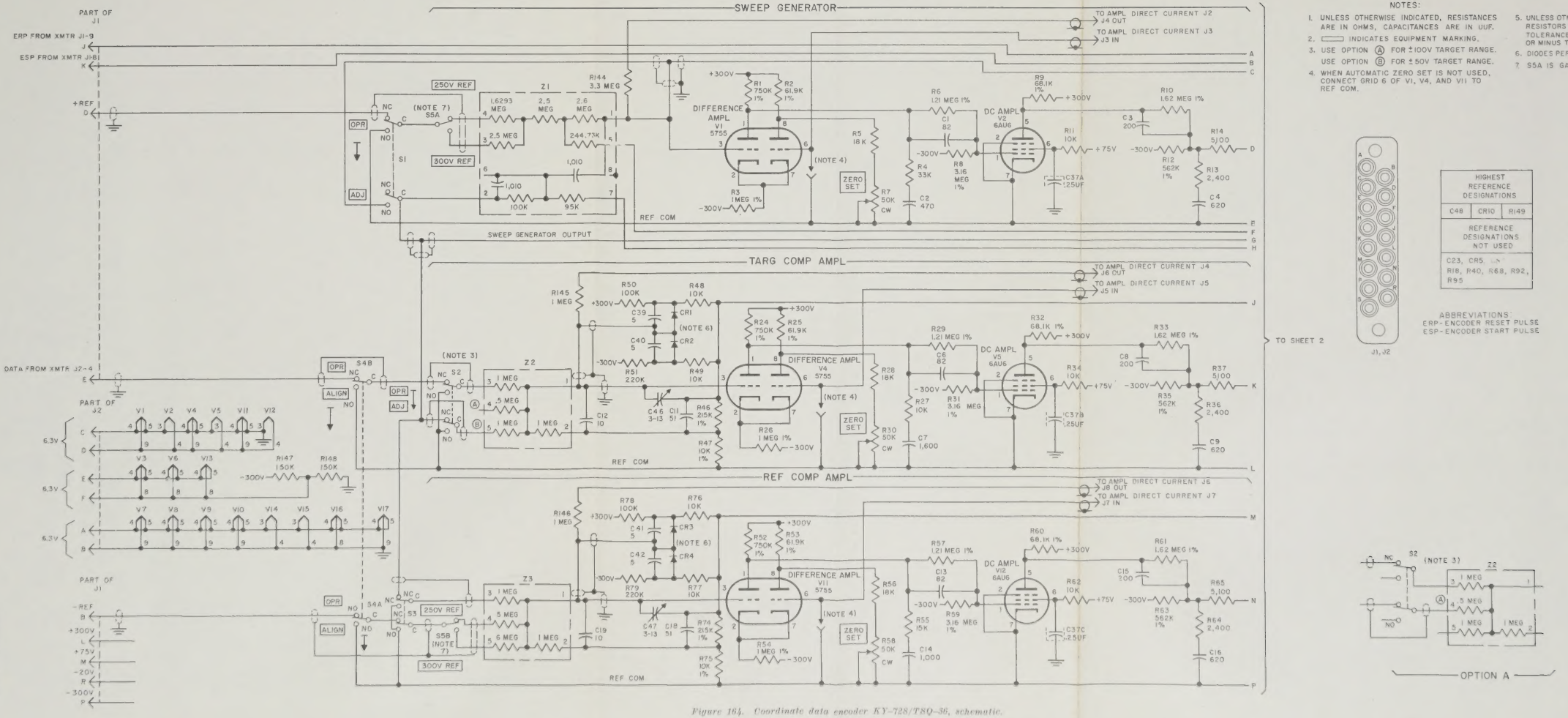


Figure 163—Continued.



NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. ▭ INDICATES EQUIPMENT MARKING.
3. USE OPTION (A) FOR ±100V TARGET RANGE. USE OPTION (B) FOR ±50V TARGET RANGE.
4. WHEN AUTOMATIC ZERO SET IS NOT USED, CONNECT GRID 6 OF V1, V4, AND V11 TO REF COM.
5. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±5% TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
6. DIODES PER SM-C-190480.
7. S5A IS GANGED WITH S5B.

J1, J2

HIGHEST REFERENCE DESIGNATIONS		
C48	CR10	R149
REFERENCE DESIGNATIONS NOT USED		
C23, CR5, CR7, R18, R40, R68, R92, R95		

ABBREVIATIONS:
ERP-ENCODER RESET PULSE
ESP-ENCODER START PULSE

Figure 164. Coordinate data encoder KY-728/TSQ-36, schematic.

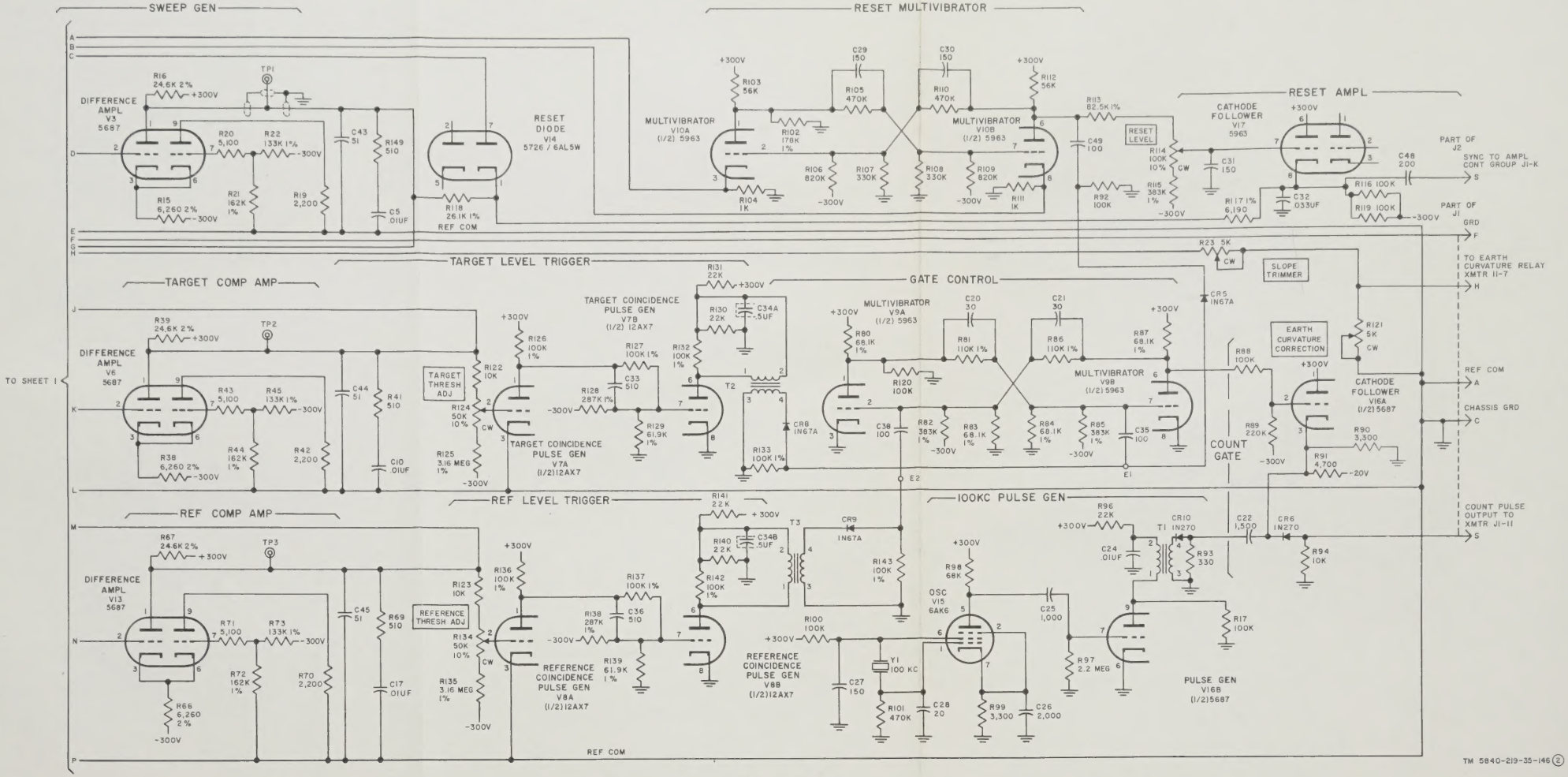
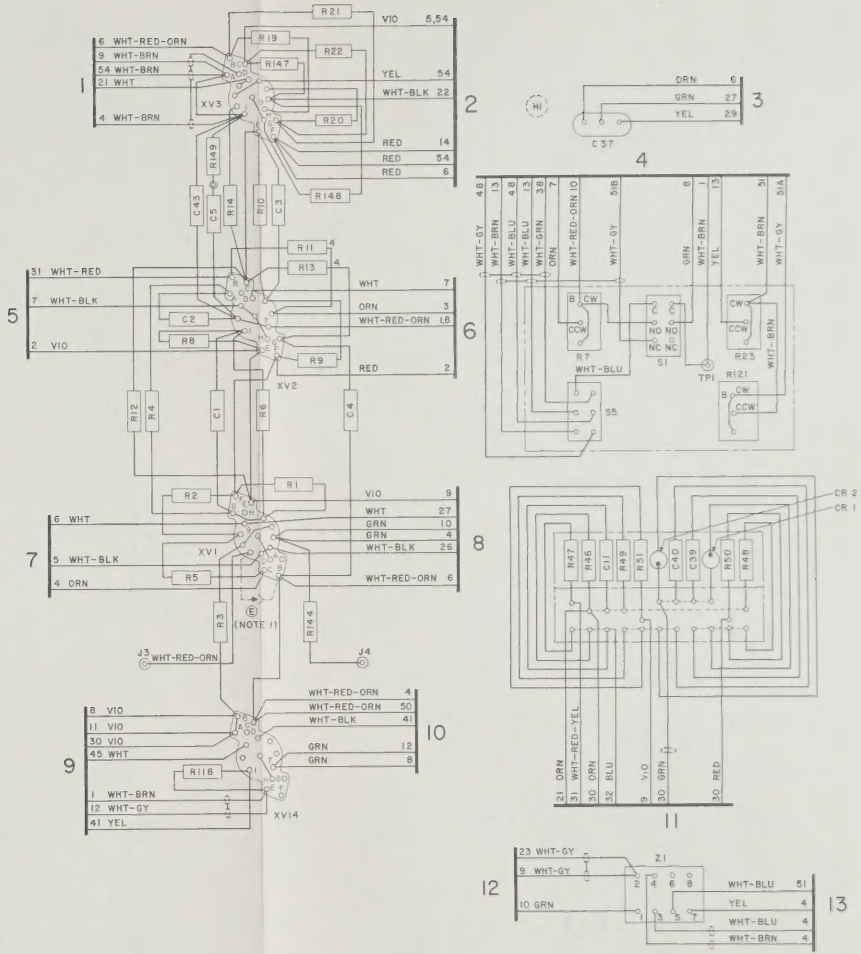


Figure 164—Continued.



NOTE:
FURNISH OPTION (E) ONLY WHEN THE GS-17422 AMPLIFIER O.C. (AZS) IS NOT FURNISHED.

Figure 165. Coordinate data encoder KY-278/TSQ-36, wiring diagram.

504693 O - 59 (In pocket)

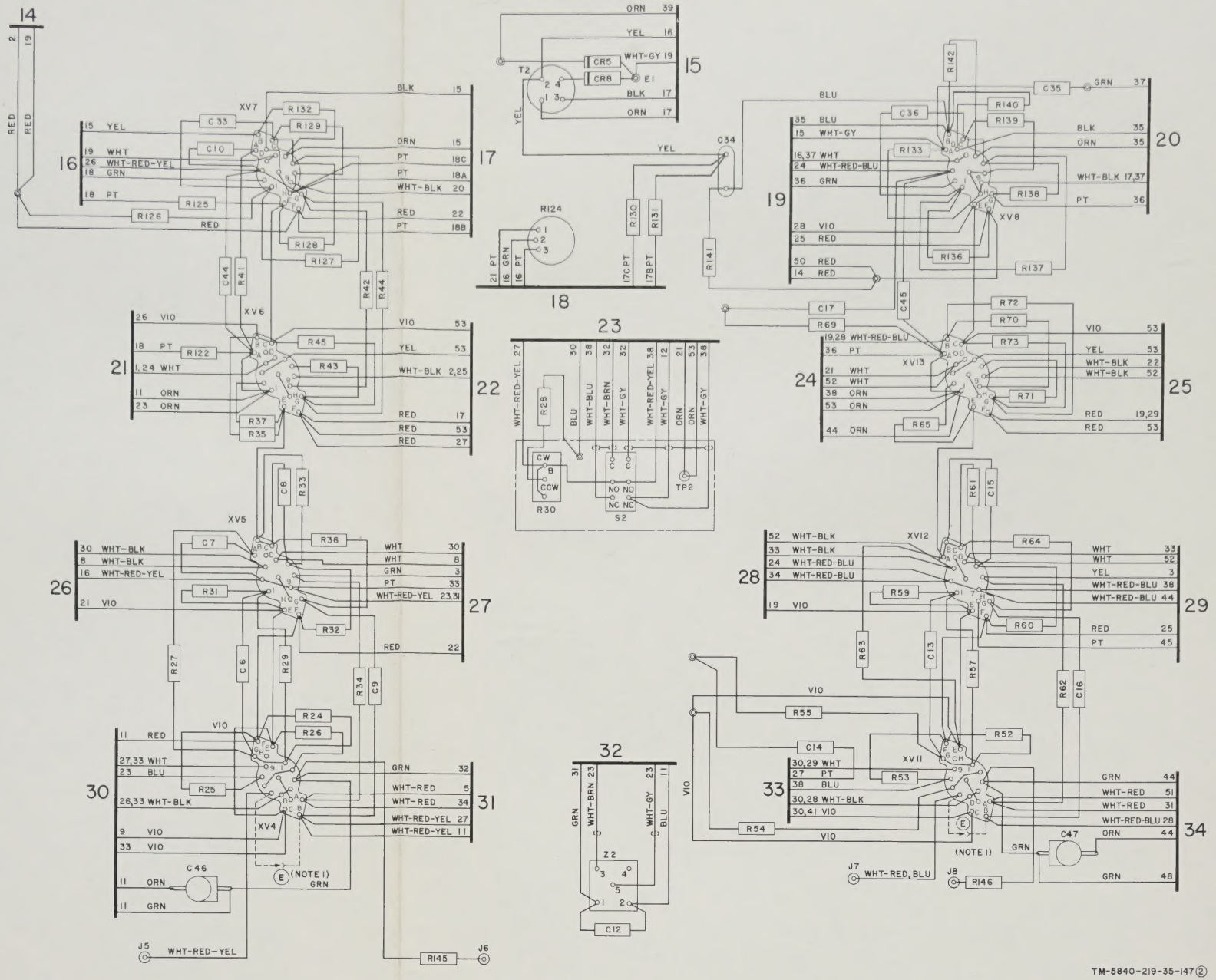


Figure 165—Continued.

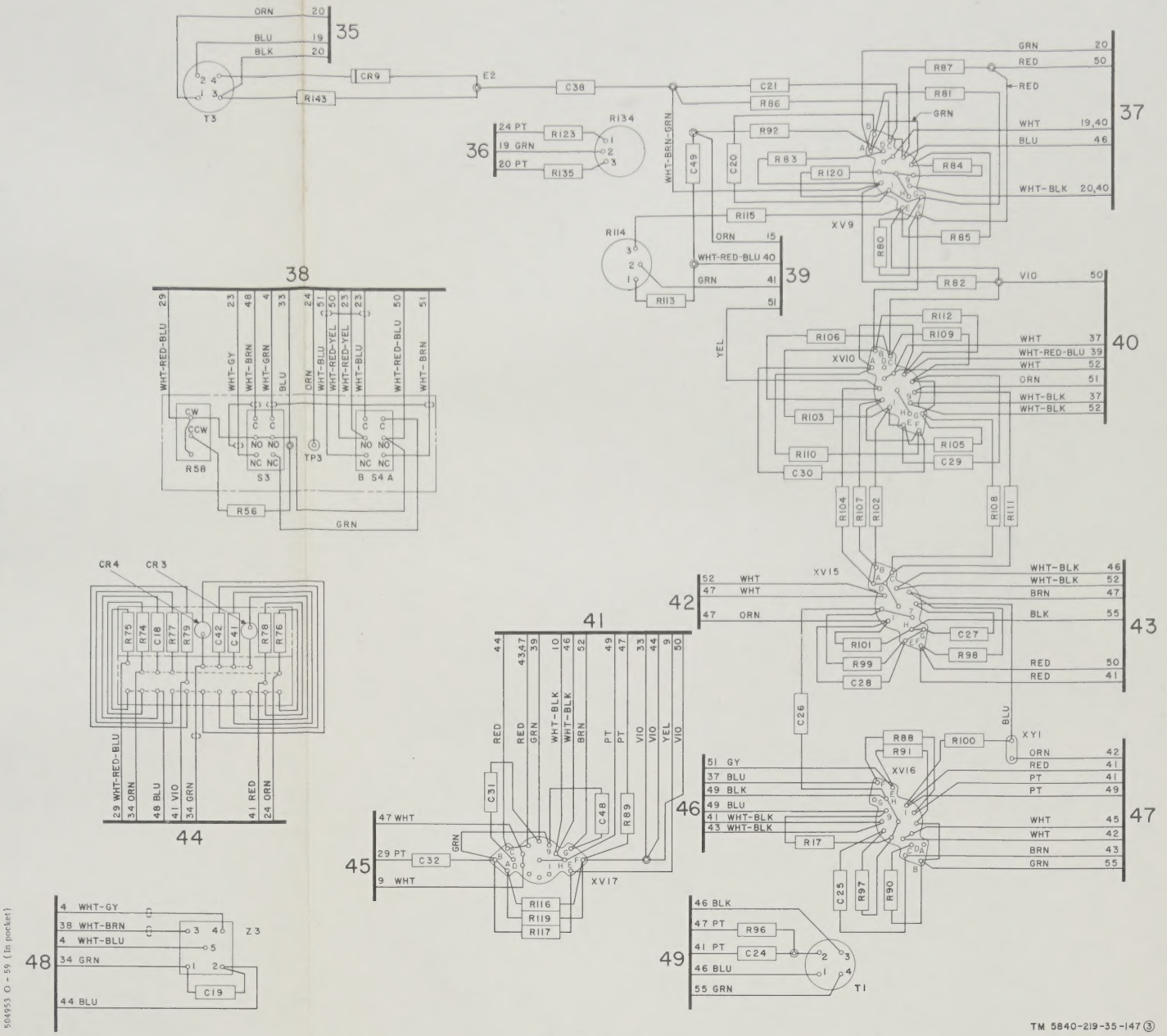
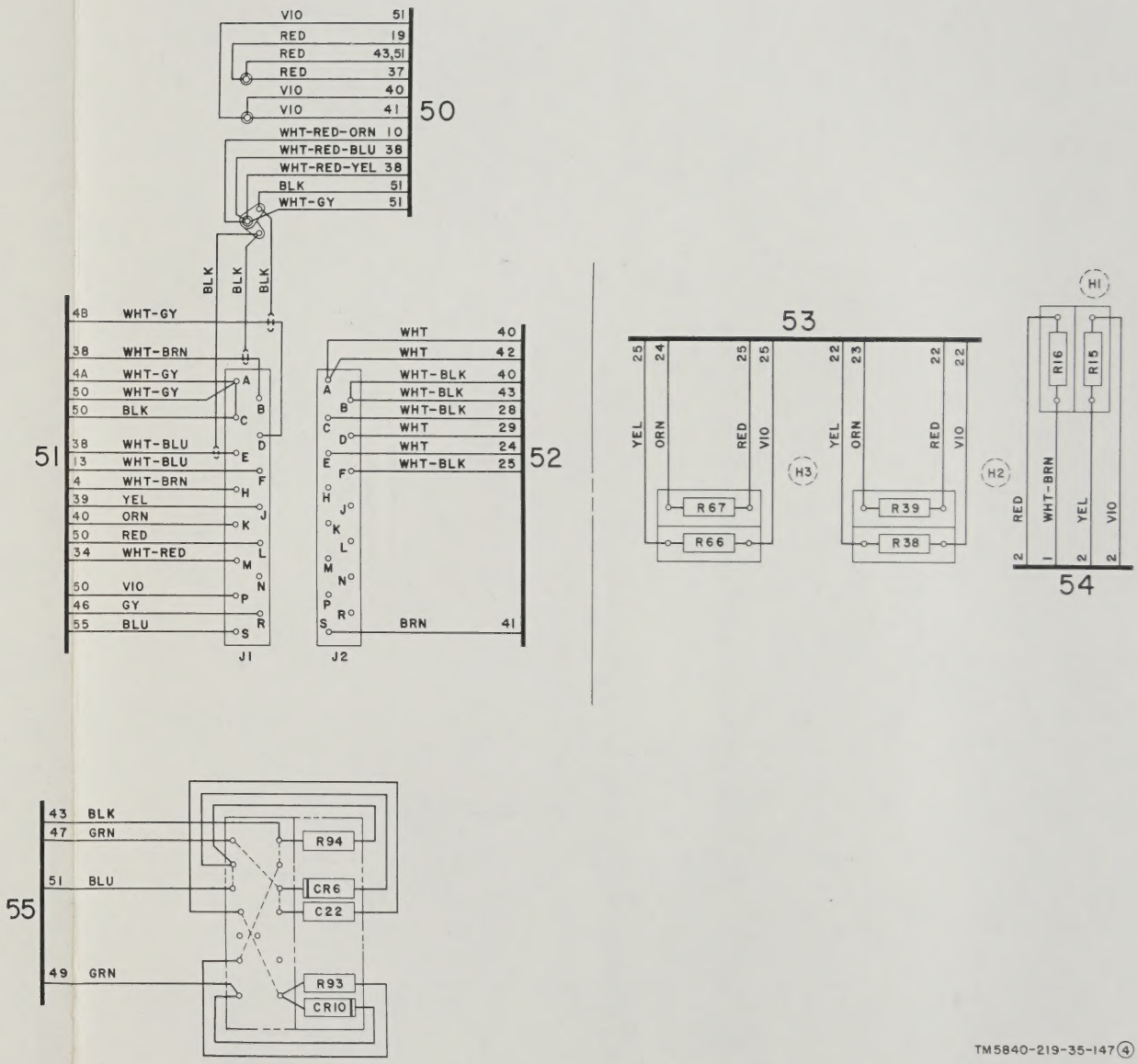


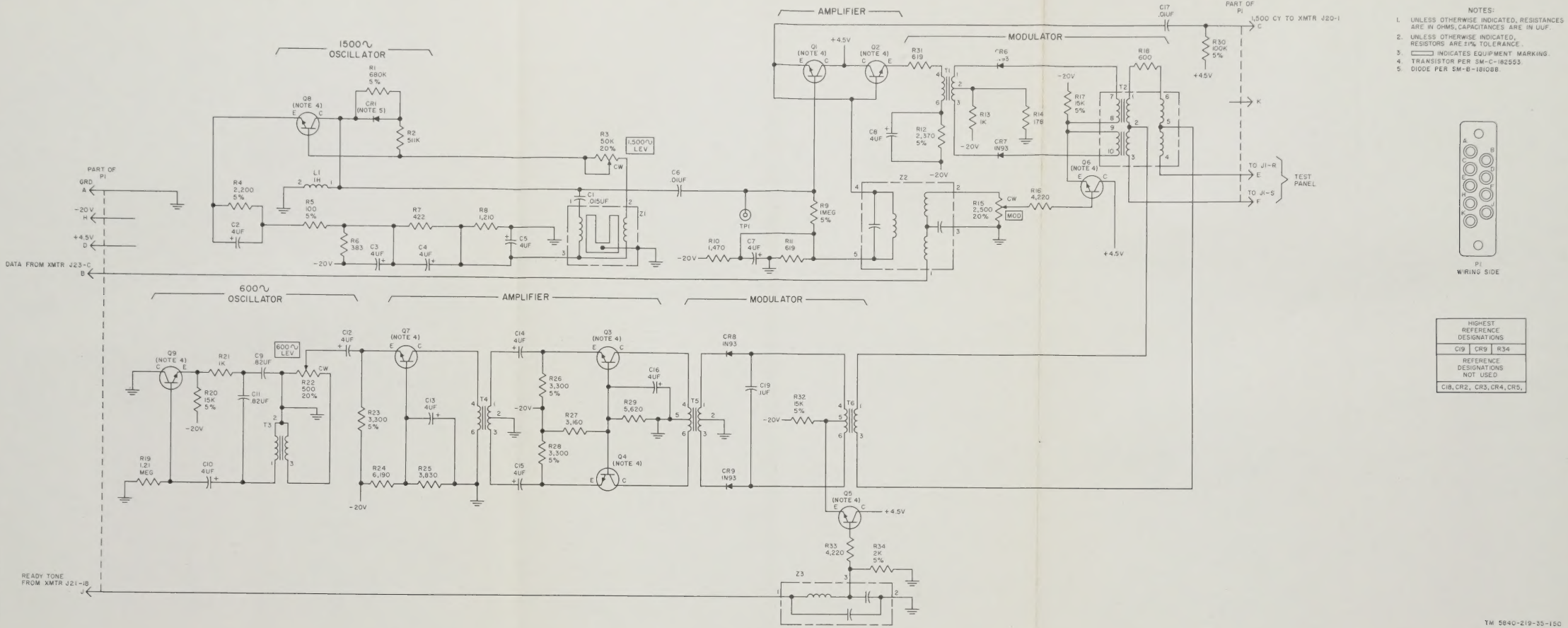
Figure 165—Continued.



TM5840-219-35-147④

Figure 165—Continued.

504953 O - 59 (In pocket)



NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±1% TOLERANCE.
3. ▭ INDICATES EQUIPMENT MARKING.
4. TRANSISTOR PER SM-C-162553.
5. DIODE PER SM-B-181088.

HIGHEST REFERENCE DESIGNATIONS		
C19	CR9	R34
REFERENCE DESIGNATIONS NOT USED		
C18, CR2, CR3, CR4, CR5,		

564913 O-59 (In pocket)

Figure 168. Coordinate data modulator MD-323A/G, schematic.

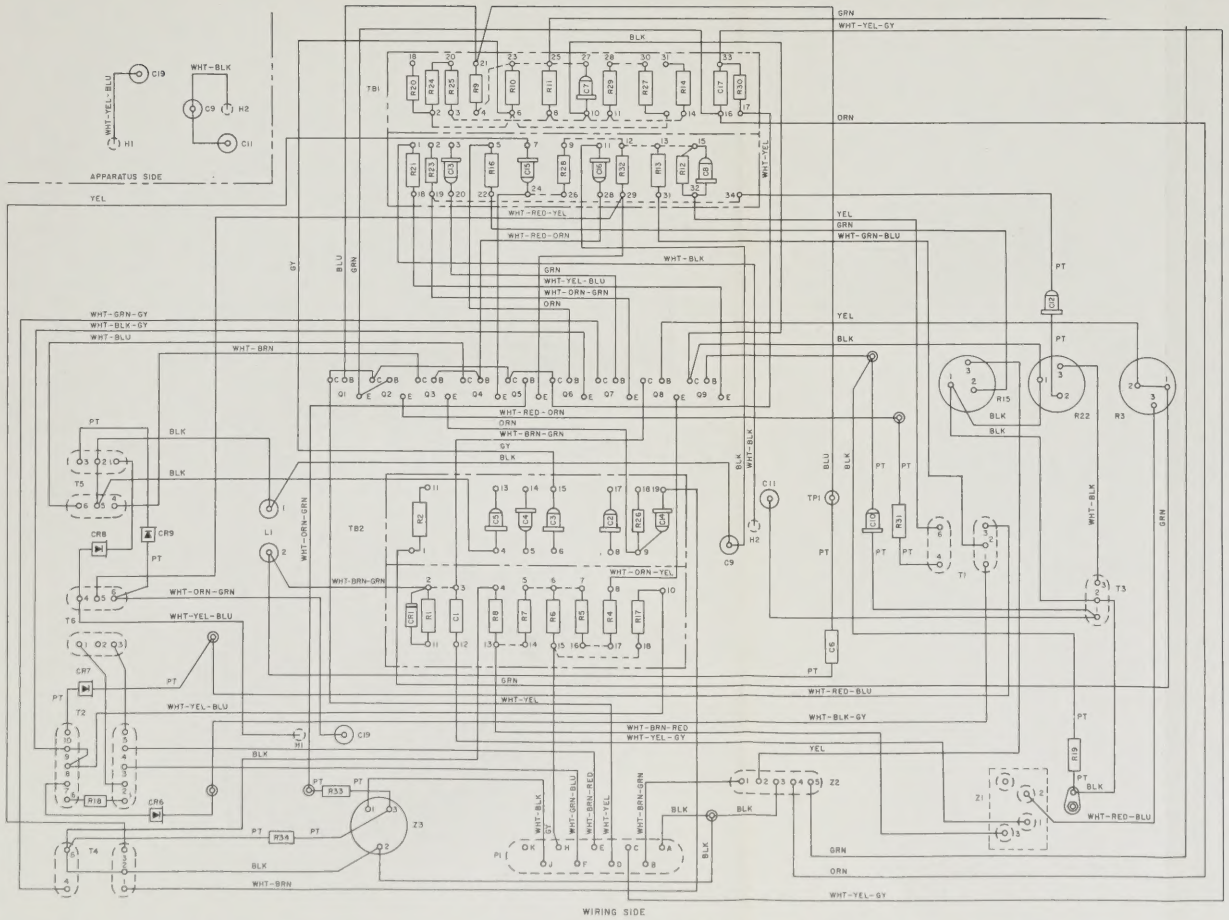


Figure 169. Coordinate data modulator MD-323A/G, wiring diagram.

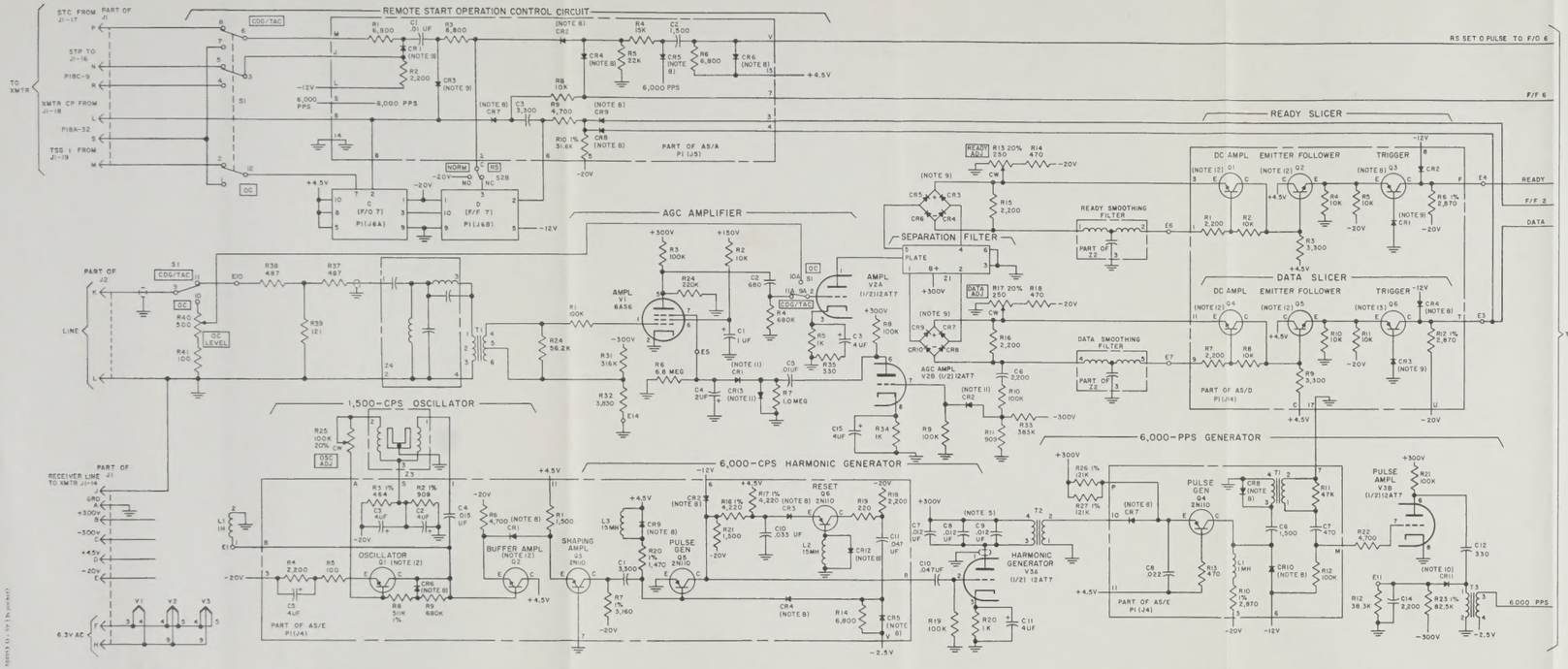


Figure 170. Amplifier-synchronizer unit AM-2126/TSQ-36, schematic.

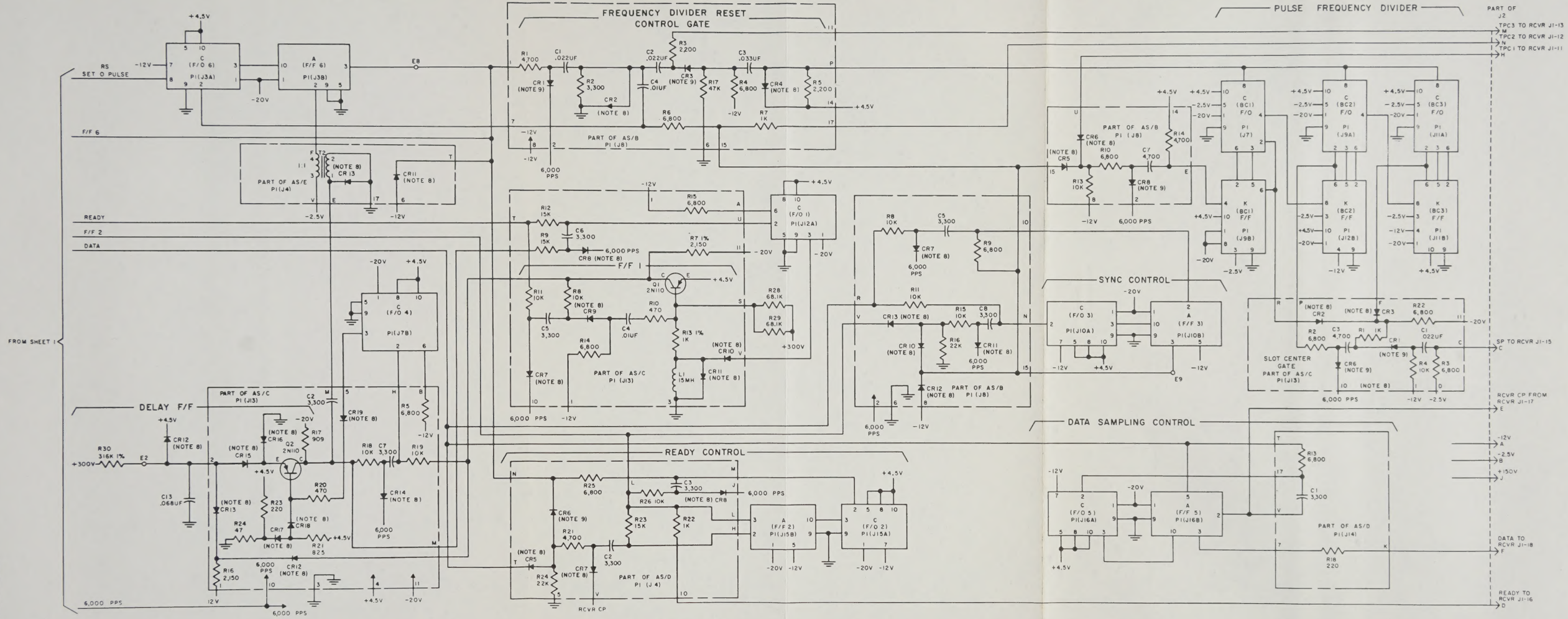


Figure 170—Continued.

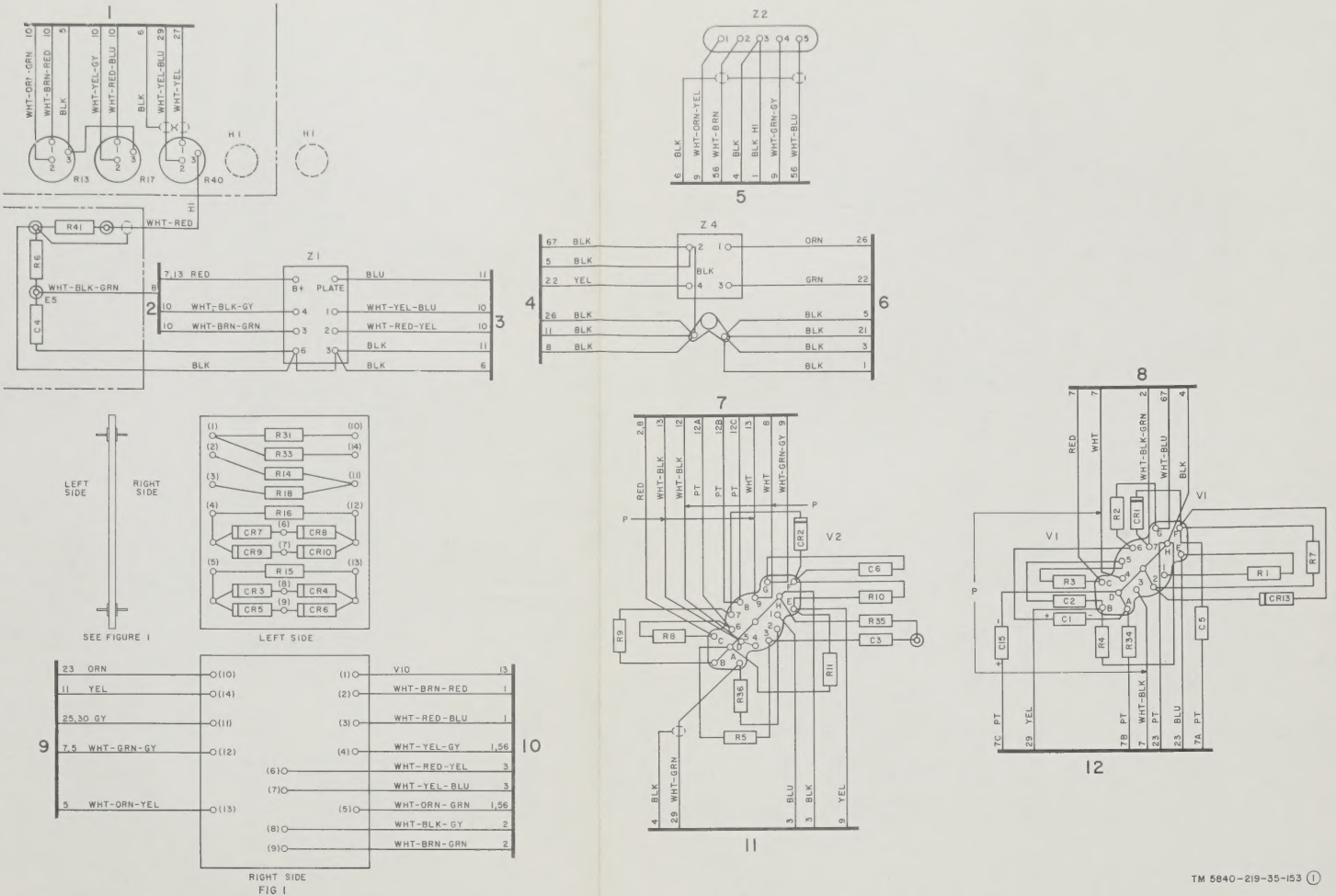


Figure 171. Amplifier-synchronizer unit AM-2126/TSQ-36, wiring diagram.

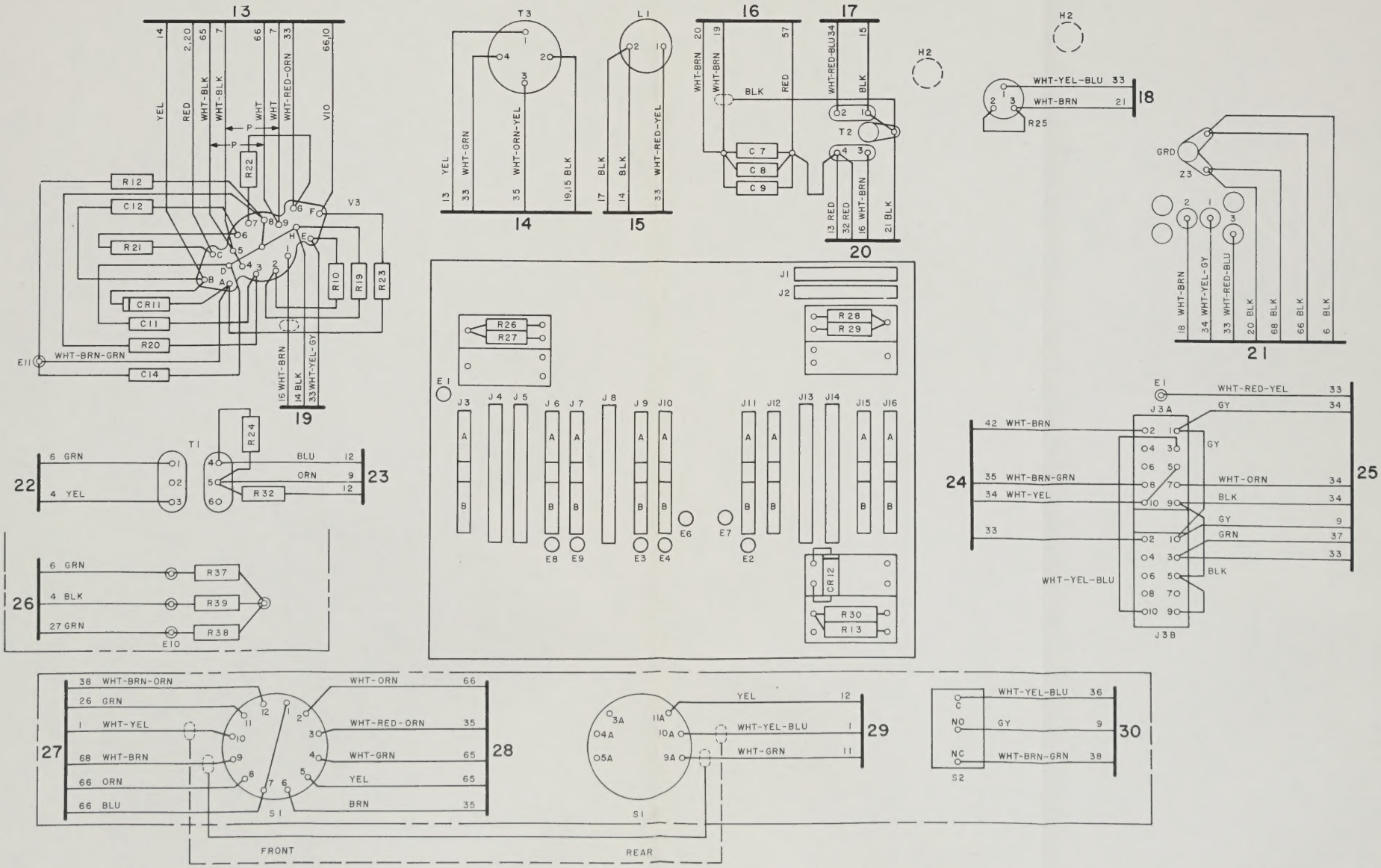
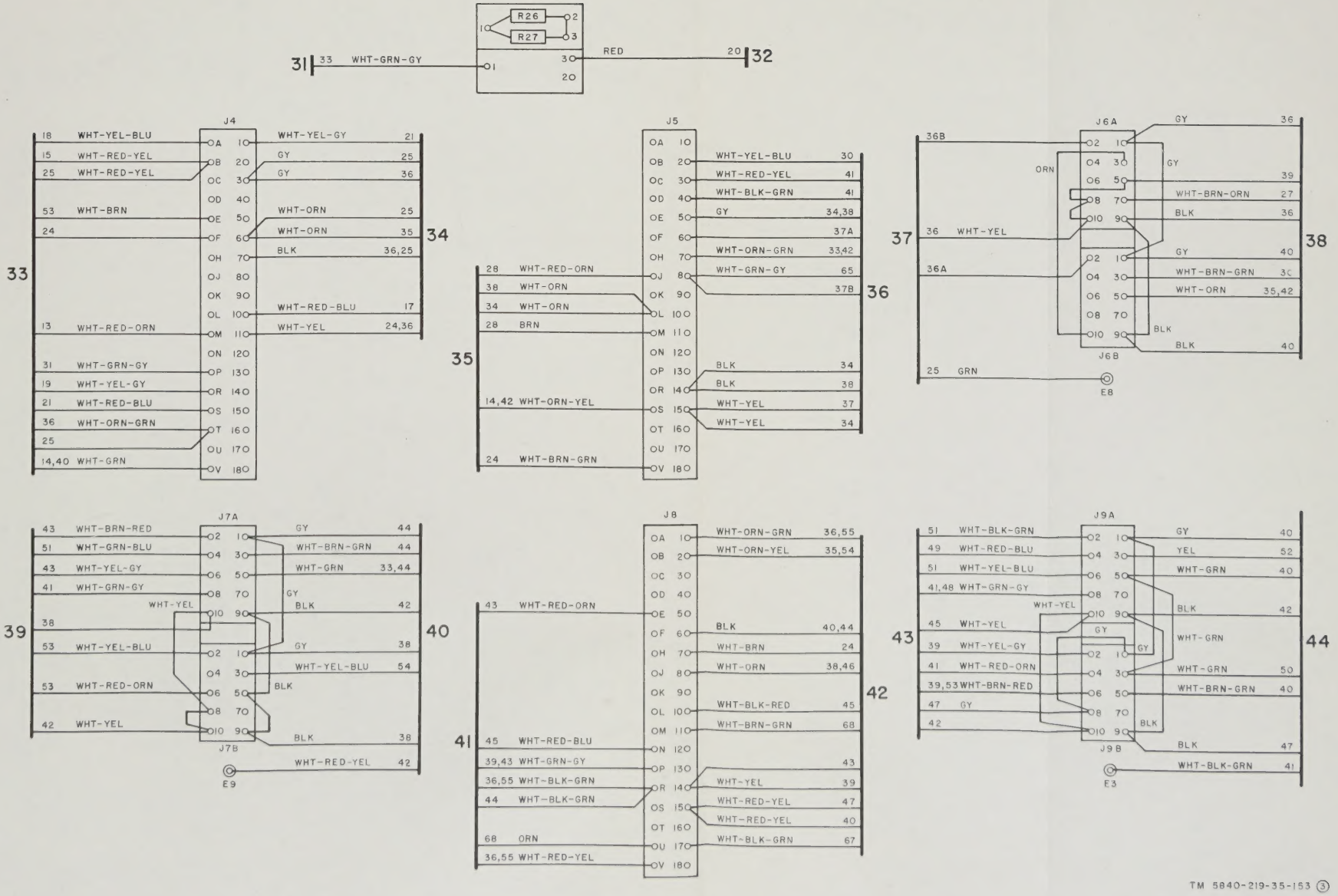


Figure 171—Continued.

504933 O - 59 (In pocket)



TM 5840-219-35-153 ③

504953 O - 59 (In pocket)

Figure 171—Continued.

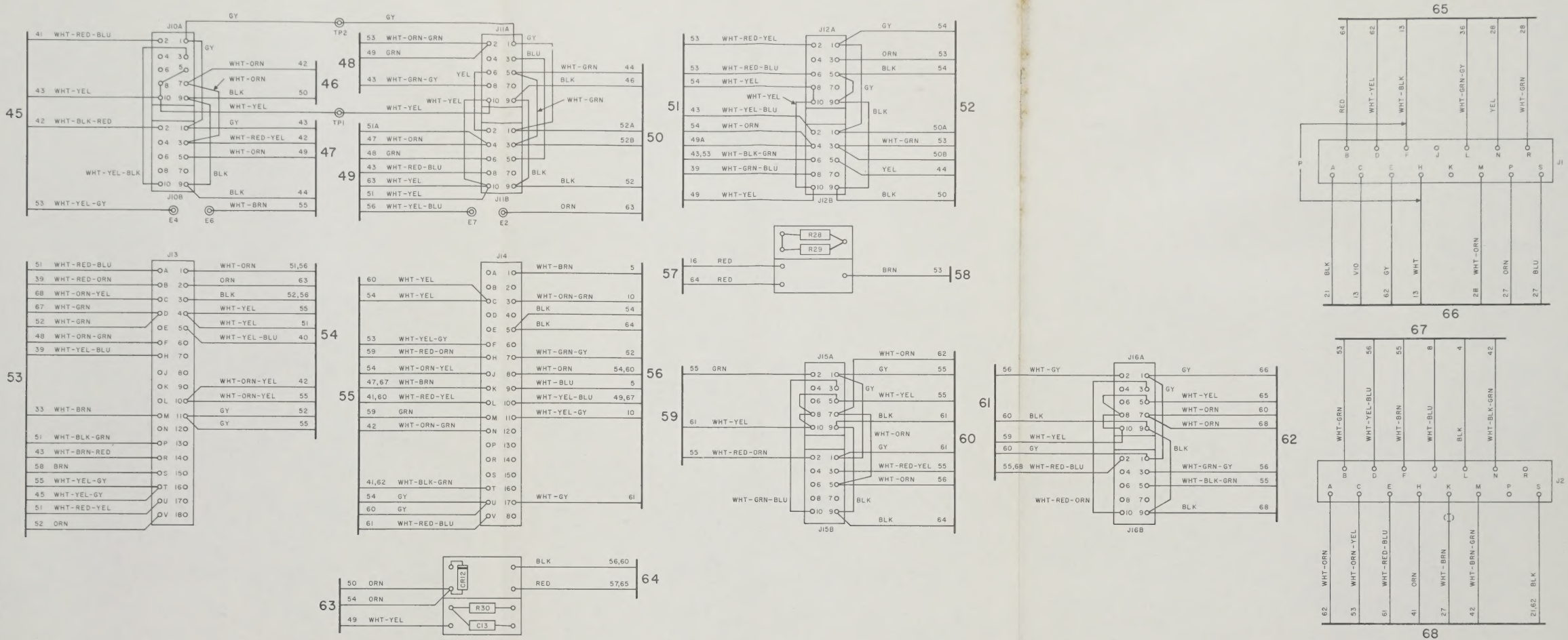


Figure 171—Continued.

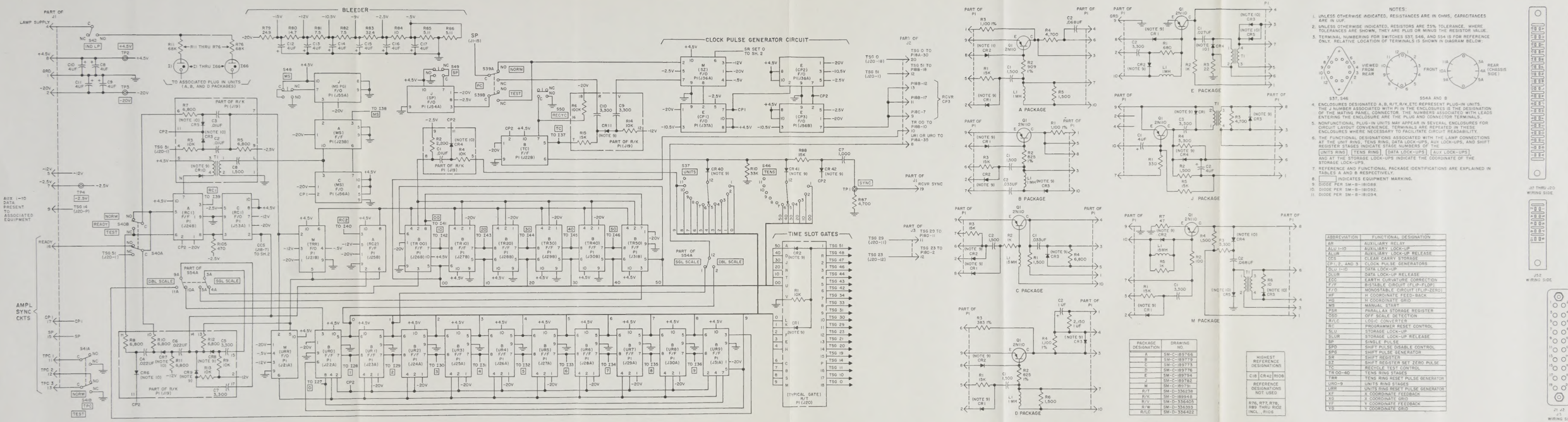

BLEEDER
CLOCK PULSE GENERATOR CIRCUIT
TIME SLOT GATES
AMPL SYNC CKTS
AUX I-10 DATA PRESENT TO ASSOCIATED EQUIPMENT
TO ASSOCIATED PLUG IN UNITS (A, B, AND D PACKAGES)
SP (J-151)
RCVR CP3
RCVR SYNC
SYNC
UNITS
TENS
DBL SCALE
SGL SCALE
(TYPICAL GATE) R/T PI (J20)
PART OF LAMP SUPPLY J1
PART OF R/K PI (J19)
PART OF SS4A
TO 138 MS
TO 137 TC
TO 139
TO 140
TO 141
TO 142
TO 143
TO 144
TO 145
TO 146
TO 127
TO 128
TO 129
TO 130
TO 131
TO 132
TO 133
TO 134
TO 135
TO 136
TSG 0 TO PI8A-30
TSG 51 TO PI8B-18
PI8B-12
PI8B-17
PI8C-7
TR TO TO PI8A-35
URI OR URO TO PI8A-35
TSG 29 (J20-11)
TSG 23 (J20-12)
TSG 23 TO PI8D-11
TSG 29 TO PI8D-12
S37 S46
S54A AND B
A PACKAGE
B PACKAGE
C PACKAGE
D PACKAGE
E PACKAGE
J PACKAGE
M PACKAGE
NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±5% TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
3. TERMINAL NUMBERING FOR SWITCHES S37, S46, AND S54 IS FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN IN DIAGRAM BELOW.
4. ENCLOSURES DESIGNATED A, B, R/T, R/K, ETC REPRESENT PLUG-IN UNITS. THE J NUMBER ASSOCIATED WITH PI IN THE ENCLOSURES IS THE DESIGNATION OF THE MATING PANEL CONNECTOR. THE NUMBERS ASSOCIATED WITH LEADS ENTERING THE ENCLOSURE ARE THE PLUG AND CONNECTOR TERMINALS.
5. NONFUNCTIONAL PLUG-IN UNITS MAY APPEAR IN SEVERAL ENCLOSURES FOR CIRCUIT LAYOUT CONVENIENCE. TERMINALS ARE REPEATED IN THESE ENCLOSURES WHERE NECESSARY TO FACILITATE CIRCUIT READABILITY.
6. THE FUNCTIONAL DESIGNATIONS ASSOCIATED WITH THE LAMP CONNECTIONS AT THE UNIT RING, TENS RING, DATA LOCK-UPS, AUX LOCK-UPS, AND SHIFT REGISTER STAGES INDICATE STAGE NUMBERS OF THE
UNITS RING | TENS RING | DATA LOCK-UPS | AUX LOCK-UPS
AND AT THE STORAGE LOCK-UPS INDICATE THE COORDINATE OF THE STORAGE LOCK-UPS.
7. REFERENCE AND FUNCTIONAL PACKAGE IDENTIFICATIONS ARE EXPLAINED IN TABLES A AND B RESPECTIVELY.
8. [ ] INDICATES EQUIPMENT MARKING.
9. DIODE PER SM-B-181088.
10. DIODE PER SM-B-181092.
11. DIODE PER SM-B-181094.
PACKAGE DESIGNATION | DRAWING NO.
A | SM-C-189766
B | SM-C-189779
C | SM-C-189773
D | SM-C-189776
E | SM-C-189784
J | SM-C-189782
M | SM-C-189781
R/T | SM-D-336238
R/K | SM-D-189948
R/V | SM-D-336405
R/W | SM-D-336393
R/LC | SM-D-336422
HIGHEST REFERENCE DESIGNATIONS
C18 CR42 R108
REFERENCE DESIGNATIONS NOT USED
R76, R77, R78, R85 THRU R102 INCL., R106
ABBREVIATION | FUNCTIONAL DESIGNATION
AR | AUXILIARY RETURN
ALM 1-10 | AUXILIARY LOCK-UP
ALUR | AUXILIARY LOCK-UP RELEASE
CCS | CLEAR CARRY STORAGE
CP1, 2, AND 3 | CLOCK PULSE GENERATORS
DLU 1-10 | DATA LOCK-UP
DLUR | DATA LOCK-UP RELEASE
ECC | EARTH CURVATURE CORRECTION
F/F | BISTABLE CIRCUIT (FLIP-FLOP)
F/O | MONOSTABLE CIRCUIT (FLIP-ZERO)
HF | H COORDINATE FEED-BACK
HG | H COORDINATE GRID
MS | MANUAL STEP RELEASE
PSR | PARALLAX STORAGE REGISTER
OSD | OFF SCALE DETECTION
R/C | CODE CONVERTER
RC | PROGRAMMER RESET CONTROL
SLU | STORAGE LOCK-UP
SLUR | STORAGE LOCK-UP RELEASE
SP | SINGLE PULSE
SPD | SHIFT PULSE DISABLE CONTROL
SPG | SHIFT PULSE GENERATOR
SR | SHIFT REGISTER
SZ | SHIFT REGISTER SET ZERO PULSE
TC | RECYCLE TEST CONTROL
TR 00-40 | TENS RING STAGES
TRR | TENS RING RESET PULSE GENERATOR
URO-9 | UNITS RING STAGES
URR | UNITS RING RESET PULSE GENERATOR
XF | X COORDINATE FEEDBACK
XG | X COORDINATE GRID
YF | Y COORDINATE FEEDBACK
YG | Y COORDINATE GRID
J17 THRU J20 WIRING SIDE
J18 THRU J45 J53 THRU J56 WIRING SIDE
J52 WIRING SIDE
J44 THRU J51 WIRING SIDE
J1 J2 WIRING SIDE
TM 5840-219-35-154 (1)

Figure 172. Coordinate data receiver unit R-930/TSQ-36, schematic.

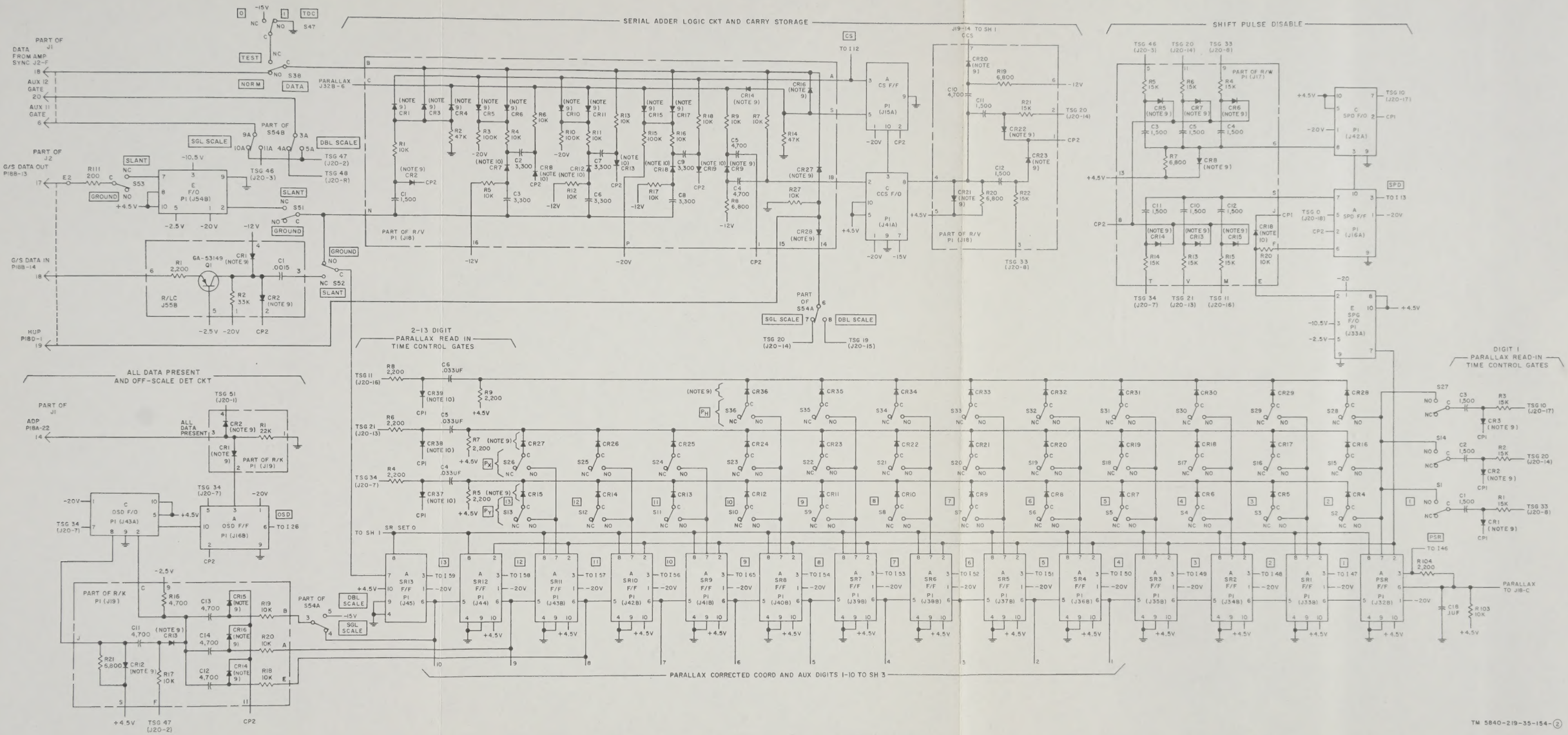


Figure 172—Continued.

504953 O - 59 (In pocket)

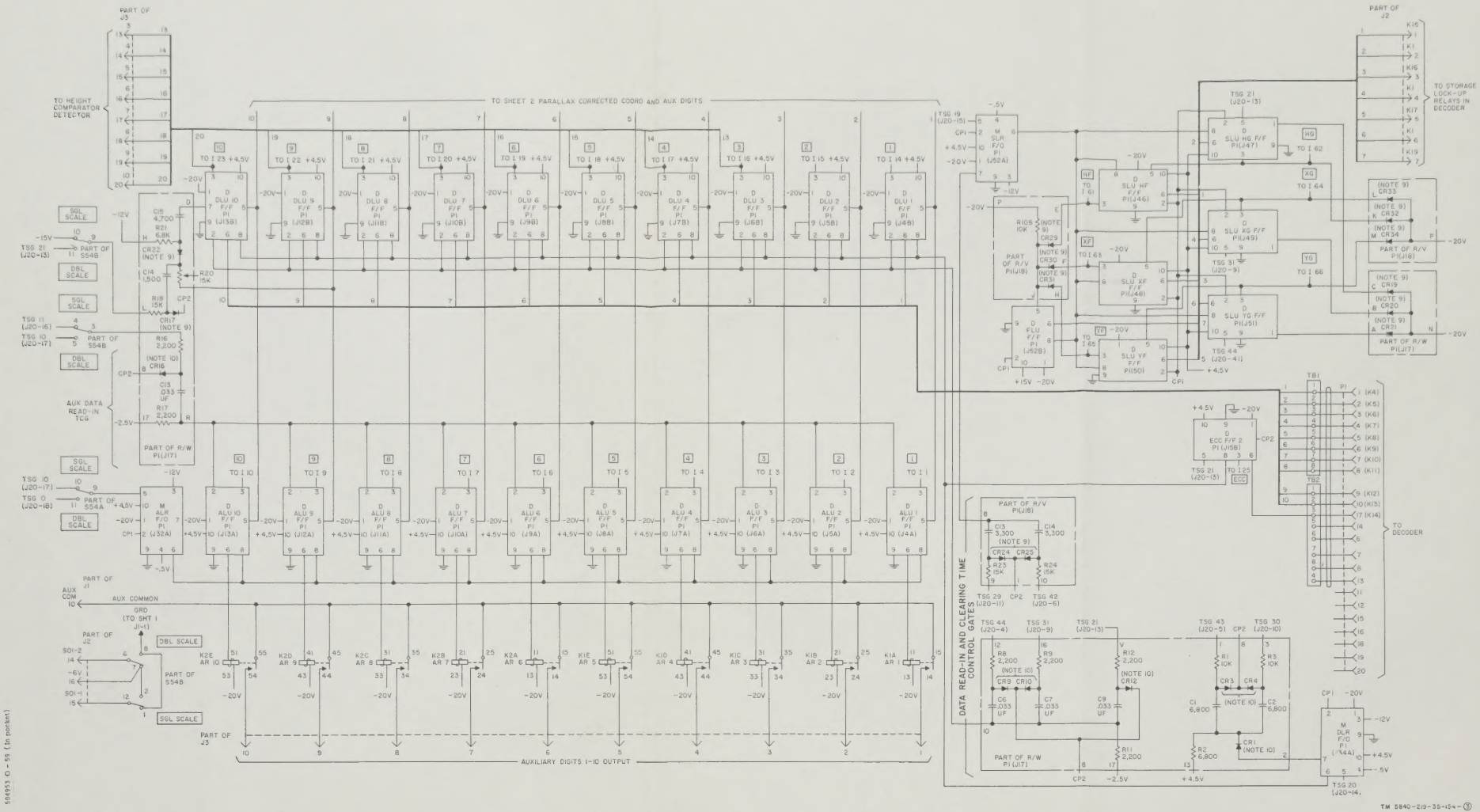


Figure 172—Continued.

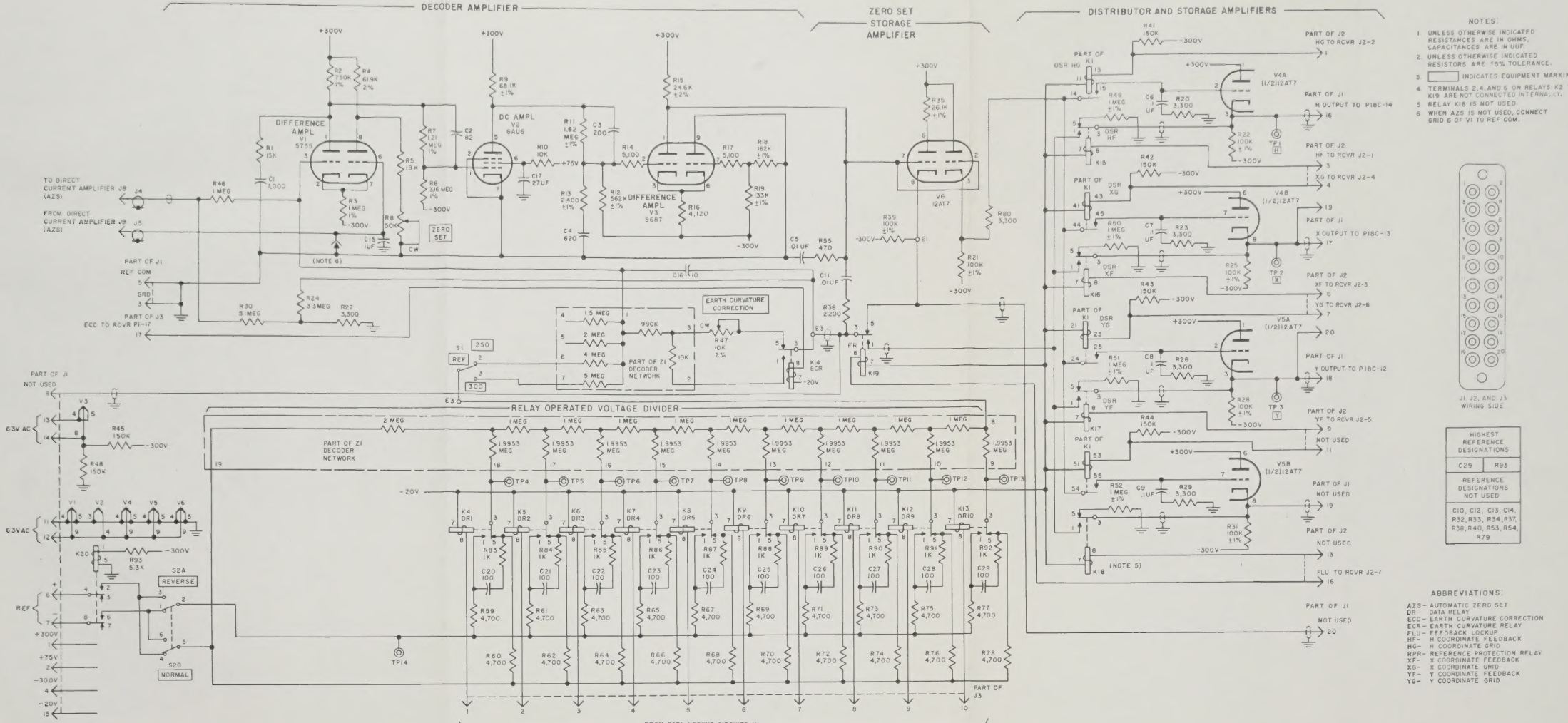

DECODER AMPLIFIER
ZERO SET STORAGE AMPLIFIER
DISTRIBUTOR AND STORAGE AMPLIFIERS
DIFFERENCE AMPL V1 5755
DC AMPL V2 6AU6
DIFFERENCE AMPL V3 5687
V6 12AT7
V4A (1/2)12AT7
V4B (1/2)12AT7
V5A (1/2)12AT7
V5B (1/2)12AT7
TO DIRECT CURRENT AMPLIFIER J8 (AZS)
FROM DIRECT CURRENT AMPLIFIER J9 (AZS)
ZERO SET
EARTH CURVATURE CORRECTION
PART OF Z1 DECODER NETWORK
RELAY OPERATED VOLTAGE DIVIDER
FROM DATA LOCKUP CIRCUITS IN RECEIVER UNIT
PART OF J3
PART OF J1
PART OF J2
REVERSE
NORMAL
S2A
S2B
63V AC
REF
+300V
+75V
-300V
-20V
NOTES:
1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED RESISTORS ARE ±5% TOLERANCE.
3. [ ] INDICATES EQUIPMENT MARKING.
4. TERMINALS 2, 4, AND 6 ON RELAYS K2 TO K19 ARE NOT CONNECTED INTERNALLY.
5. RELAY K18 IS NOT USED.
6. WHEN AZS IS NOT USED, CONNECT GRID 6 OF V1 TO REF COM.
J1, J2, AND J3 WIRING SIDE
HIGHEST REFERENCE DESIGNATIONS
C29 R93
REFERENCE DESIGNATIONS NOT USED
C10, C12, C13, C14, R32, R33, R34, R37, R38, R40, R53, R54, R79
ABBREVIATIONS:
AZS- AUTOMATIC ZERO SET
DR- DATA RELAY
ECC- EARTH CURVATURE CORRECTION
ECR- EARTH CURVATURE RELAY
FLU- FEEDBACK LOCKUP
HF- H COORDINATE FEEDBACK
HG- H COORDINATE GRID
RPR- REFERENCE PROTECTION RELAY
XF- X COORDINATE FEEDBACK
XG- X COORDINATE GRID
YF- Y COORDINATE FEEDBACK
YG- Y COORDINATE GRID
504953 O - 59 (In pocket)
TM 5840-219-35-155

Figure 173. Coordinate data decoder KY–277/TSQ–36, schematic.

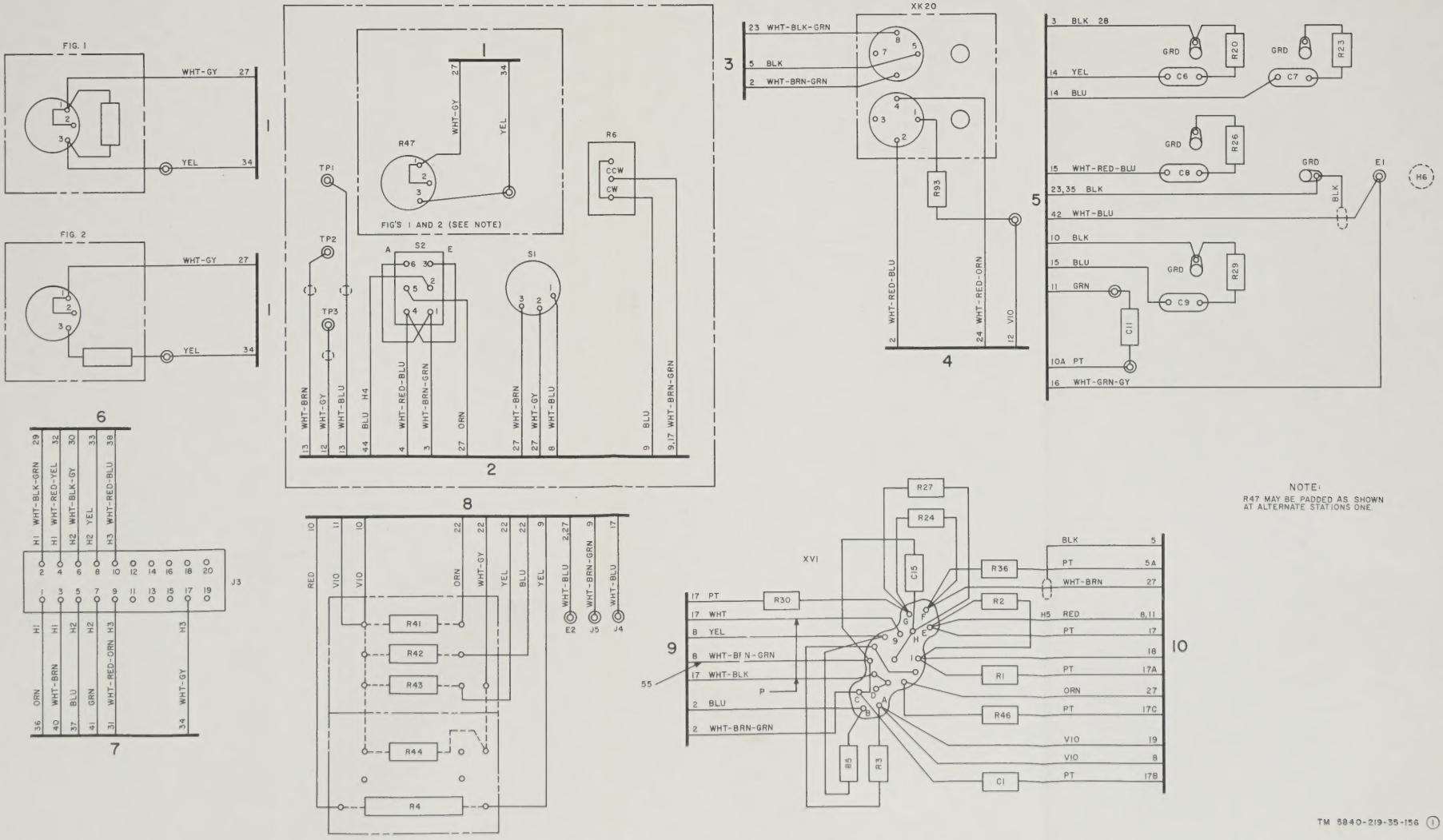


Figure 174. Coordinate data decoder KY-277/TSQ-36, wiring diagram.

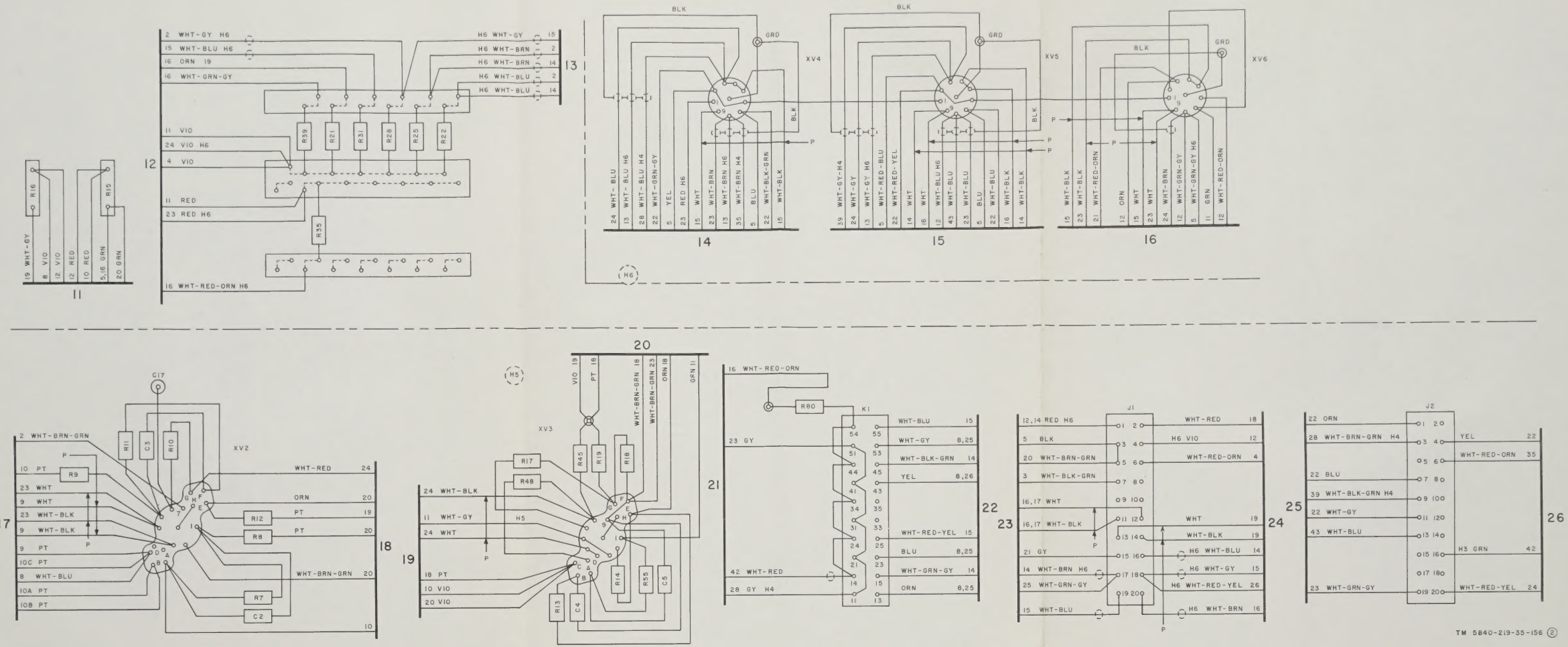


Figure 174—Continued.

504955 O - 59 (To pocket)

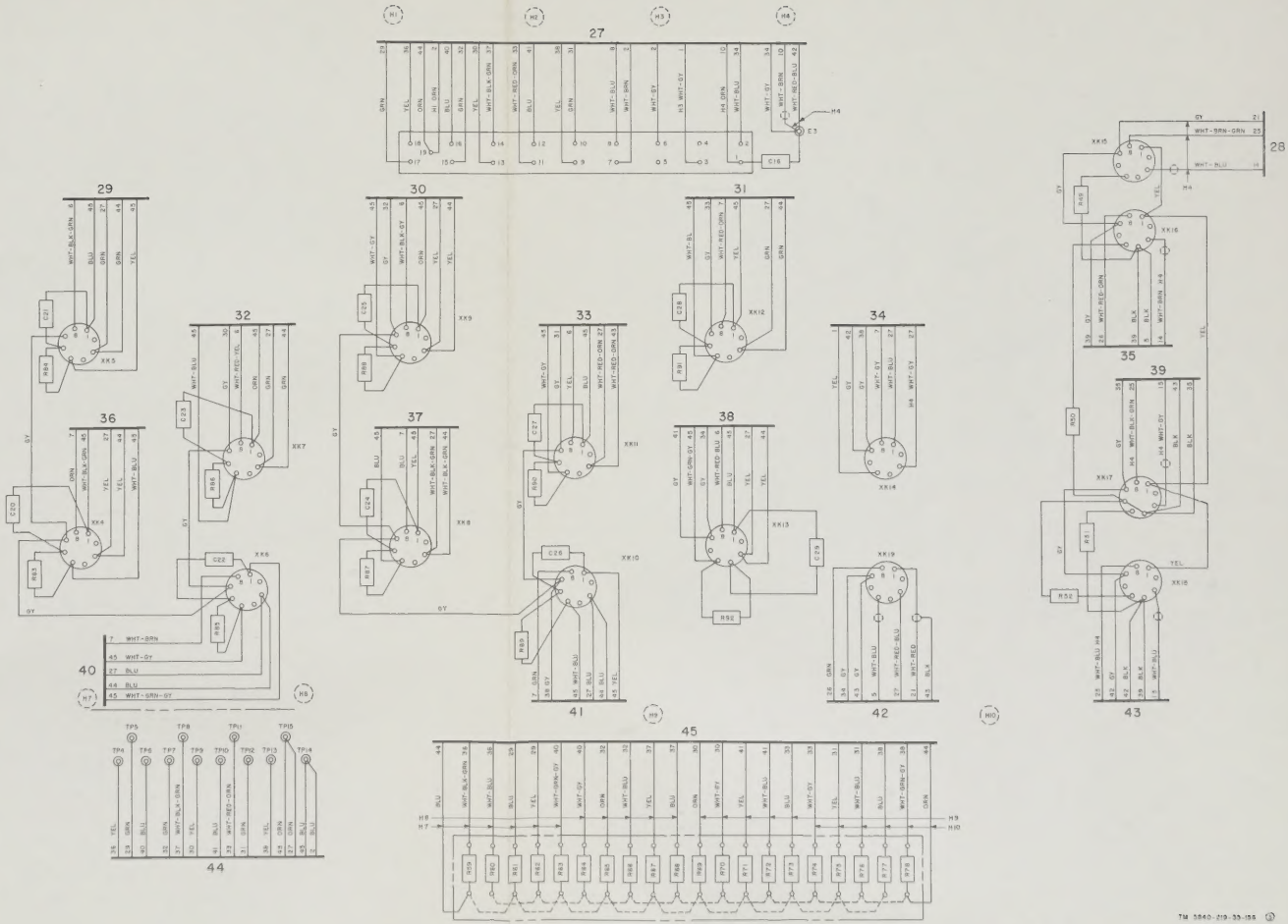
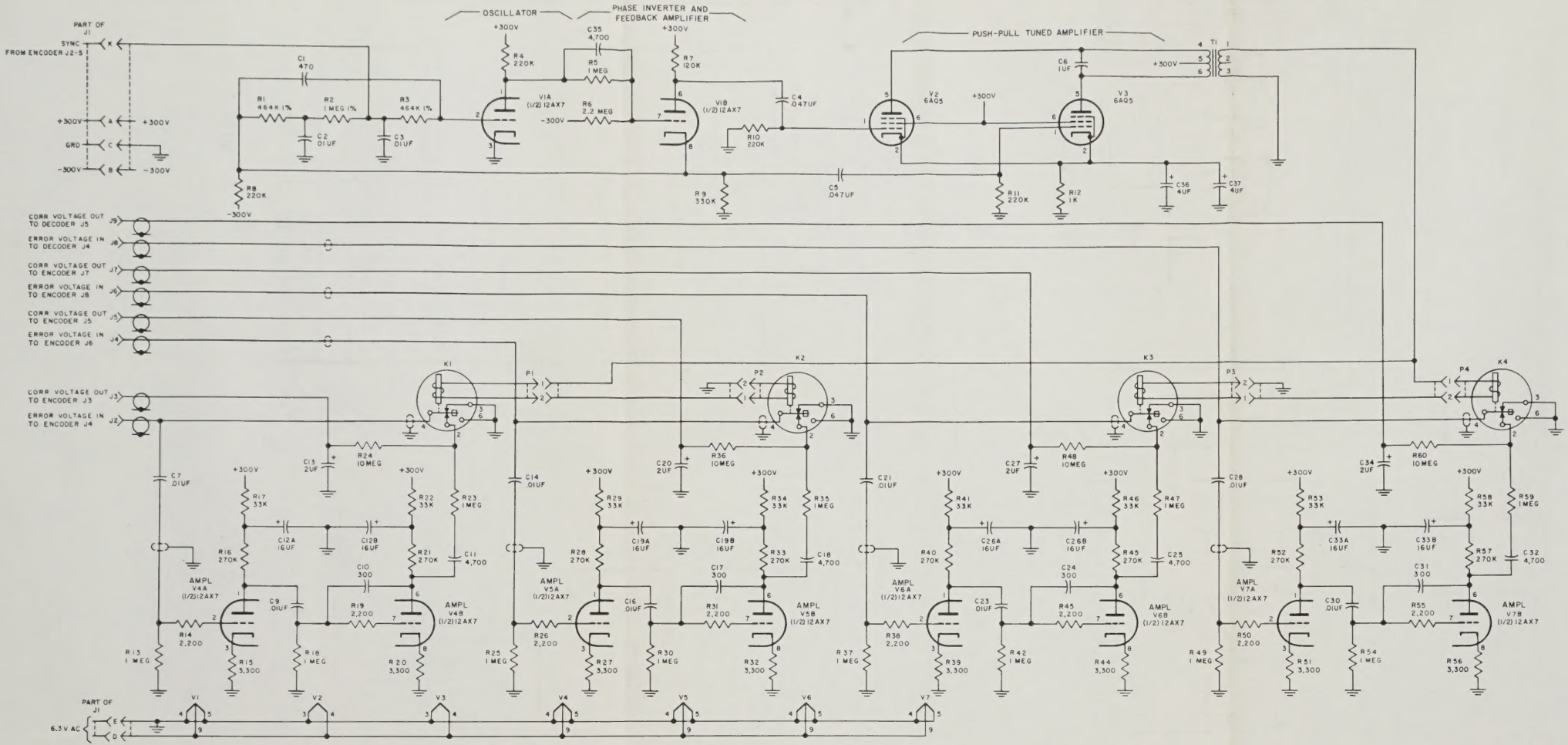


Figure 174—Continued.



NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±5% TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.

HIGHEST REFERENCE DESIGNATIONS	
C35	R61
REFERENCE DESIGNATIONS NOT USED	
C8, C15, C22, C29	

TM 5840-219-35-158

Figure 176. Direct current amplifier AM-2125/TSQ-36, schematic.

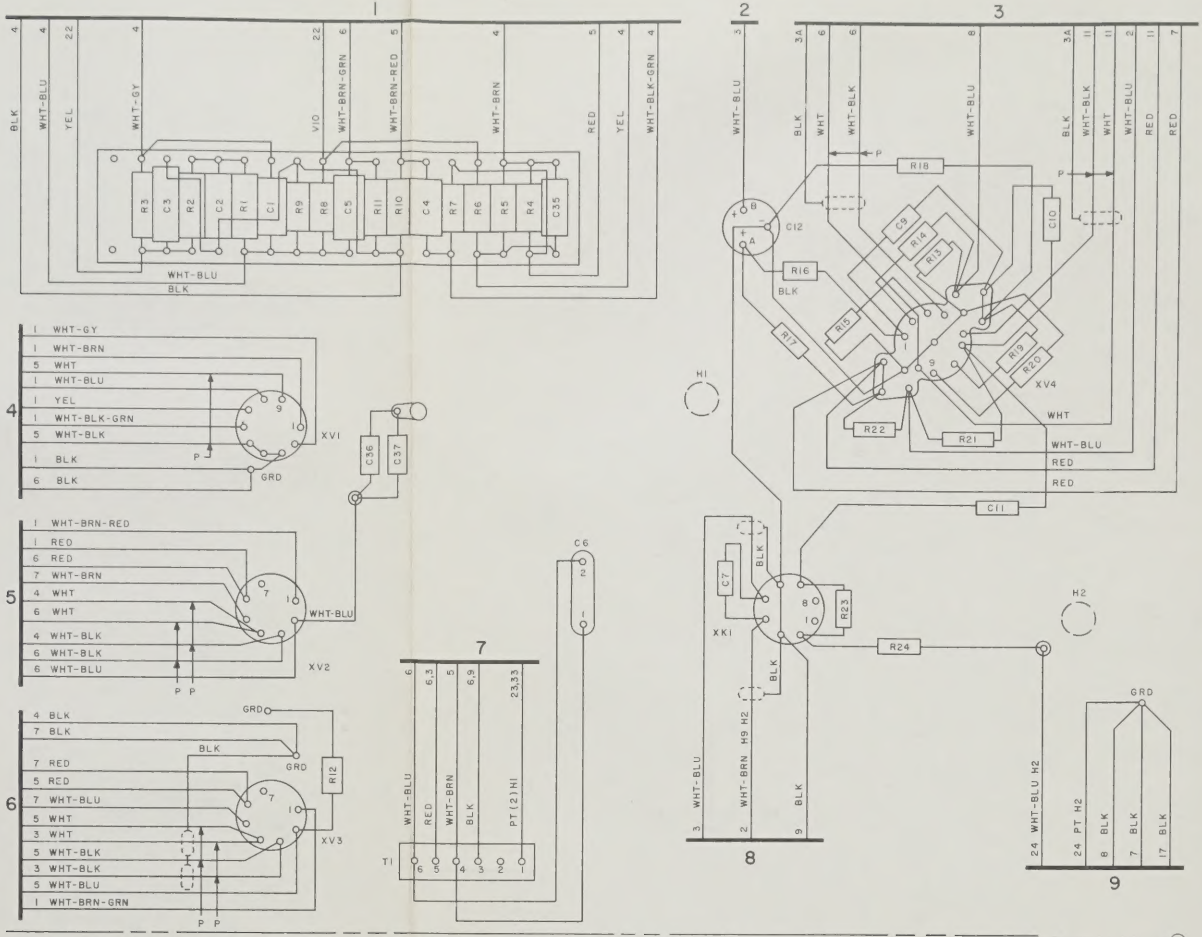
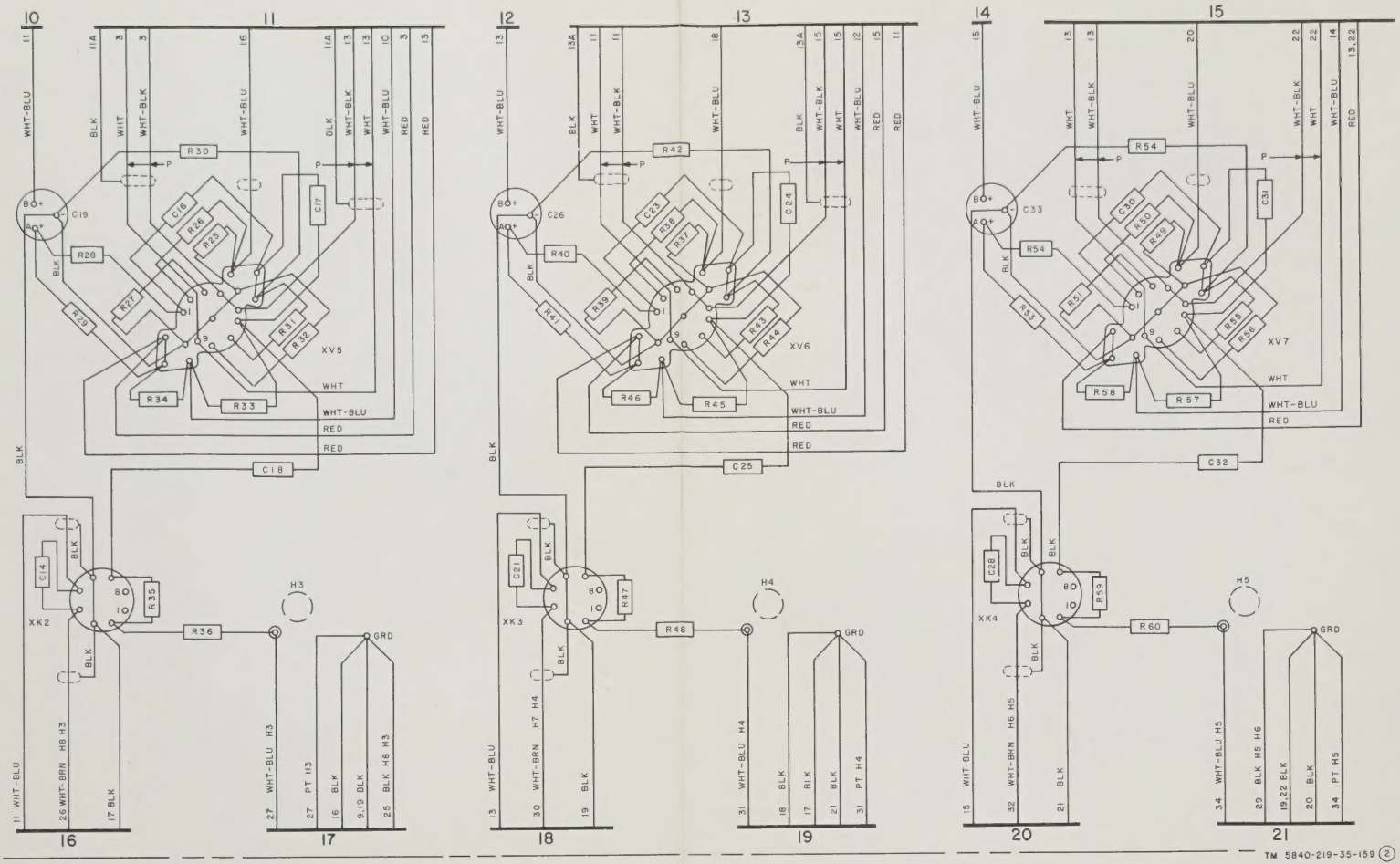
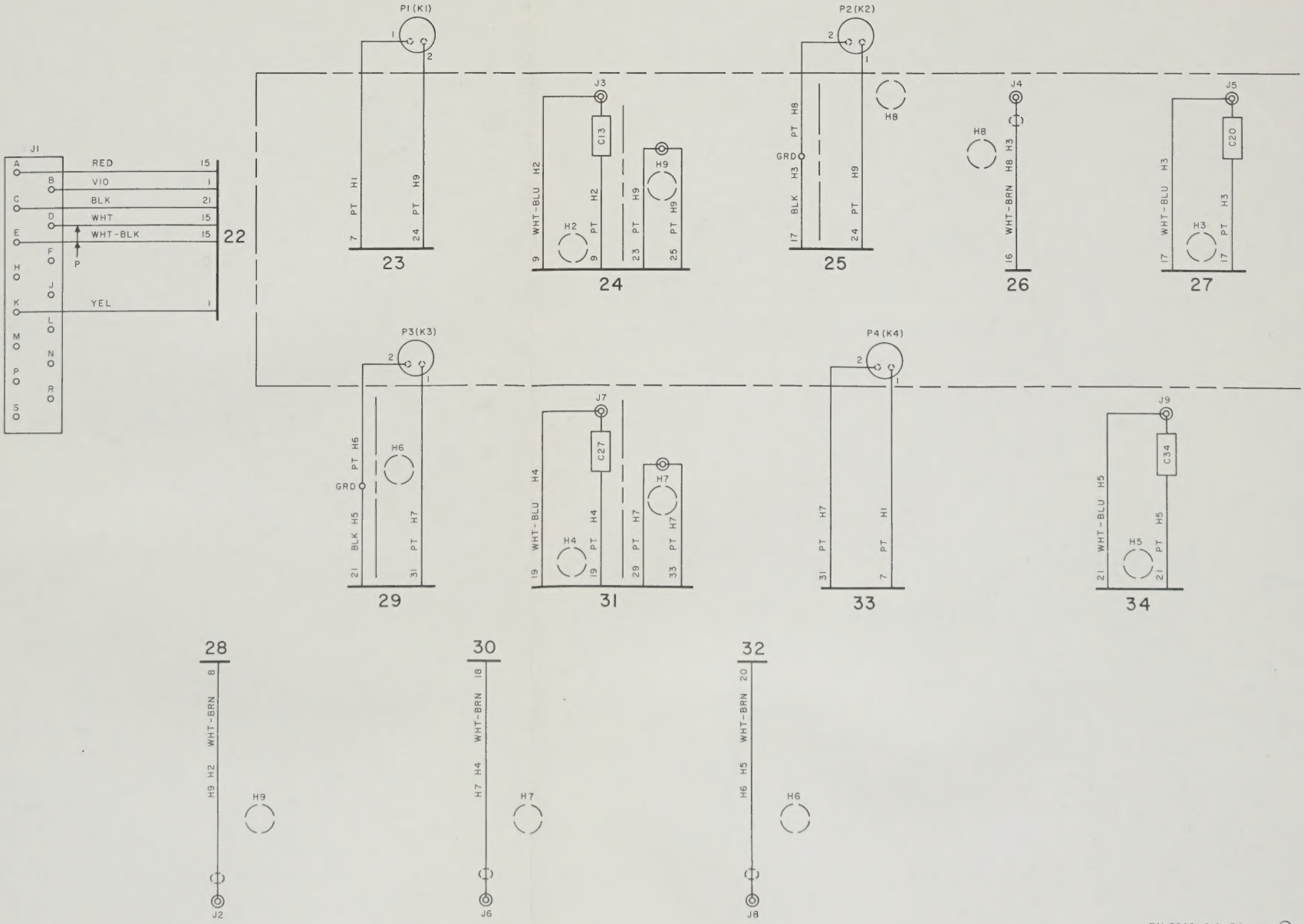


Figure 177. Direct current amplifier AM-2125/TSQ-36, wiring diagram.



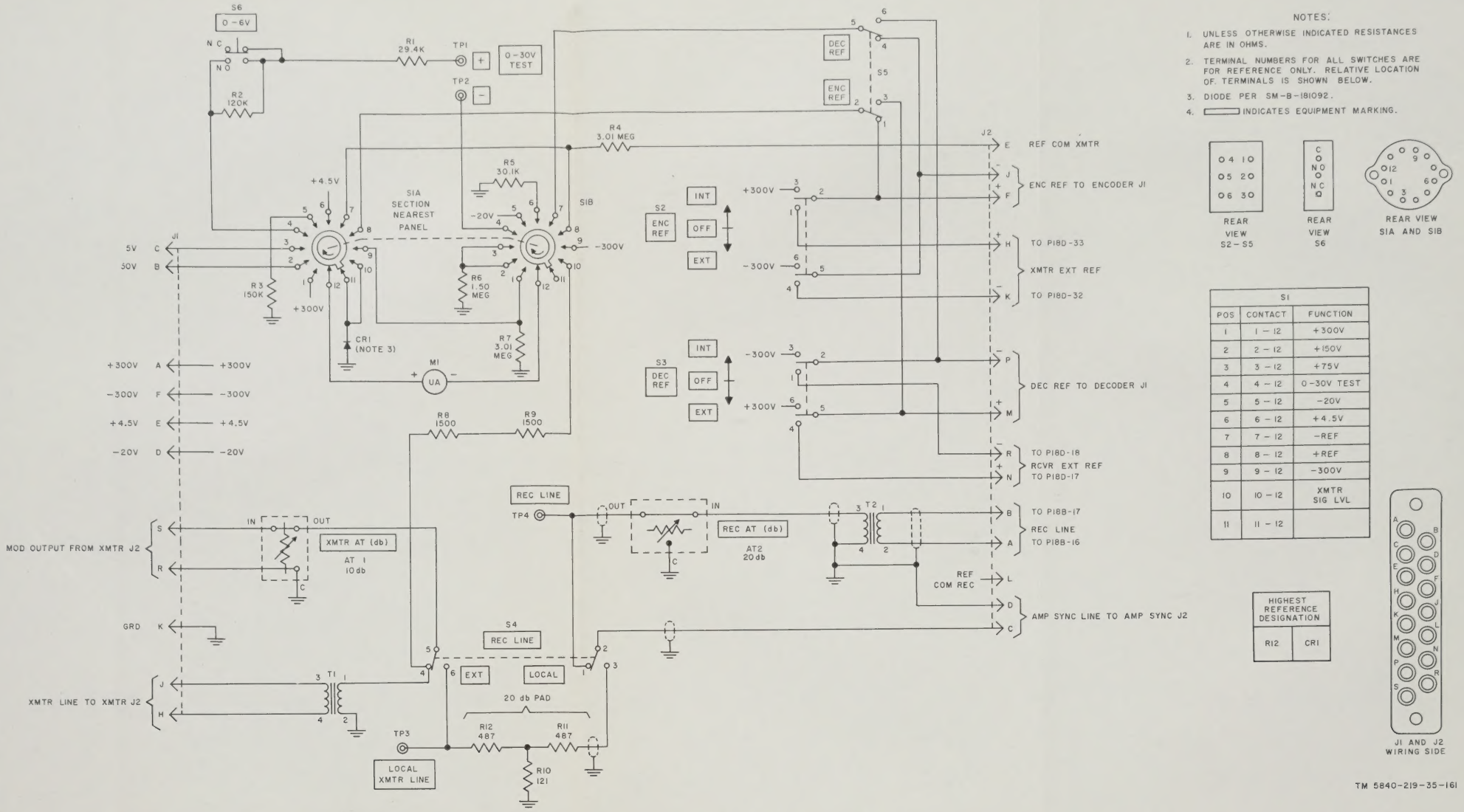
TM 5840-219-35-159 (2)

Figure 177—Continued.



504953 O - 59 (In pocket)

Figure 177—Continued.



NOTES:

1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS.
2. TERMINAL NUMBERS FOR ALL SWITCHES ARE FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN BELOW.
3. DIODE PER SM-B-181092.
4. ▭ INDICATES EQUIPMENT MARKING.

REAR VIEW S2 – S5

REAR VIEW S6

REAR VIEW SIA AND SIB

S1		
POS	CONTACT	FUNCTION
1	1 – 12	+300V
2	2 – 12	+150V
3	3 – 12	+75V
4	4 – 12	0-30V TEST
5	5 – 12	-20V
6	6 – 12	+4.5V
7	7 – 12	-REF
8	8 – 12	+REF
9	9 – 12	-300V
10	10 – 12	XMTR SIG LVL
11	11 – 12	

HIGHEST REFERENCE DESIGNATION	
R12	CR1

J1 AND J2 WIRING SIDE

TM 5840-219-35-161

504953 O - 59 (In pocket)

Figure 179. Electrical test panel SB-976/TSQ-36, schematic.

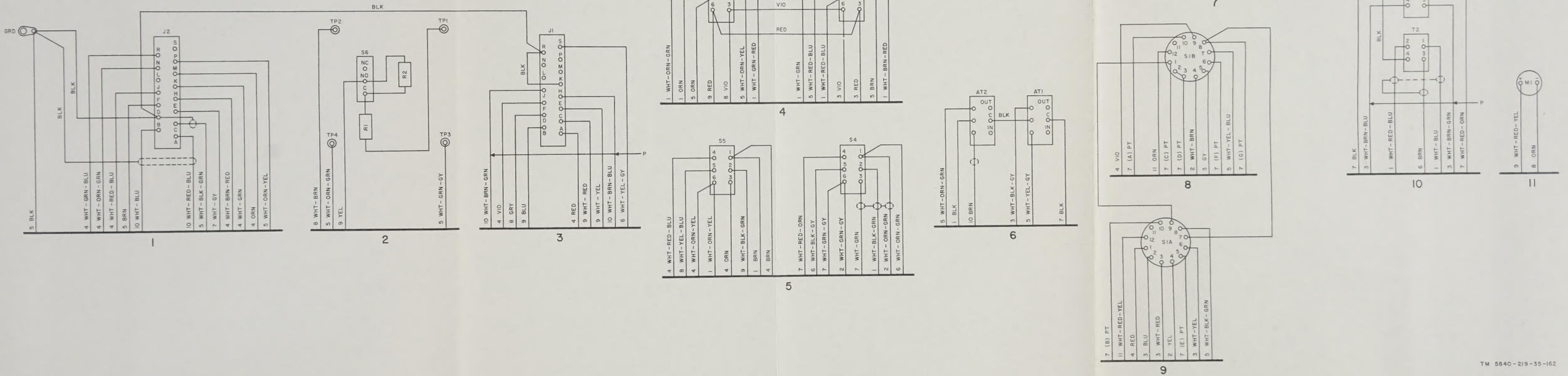
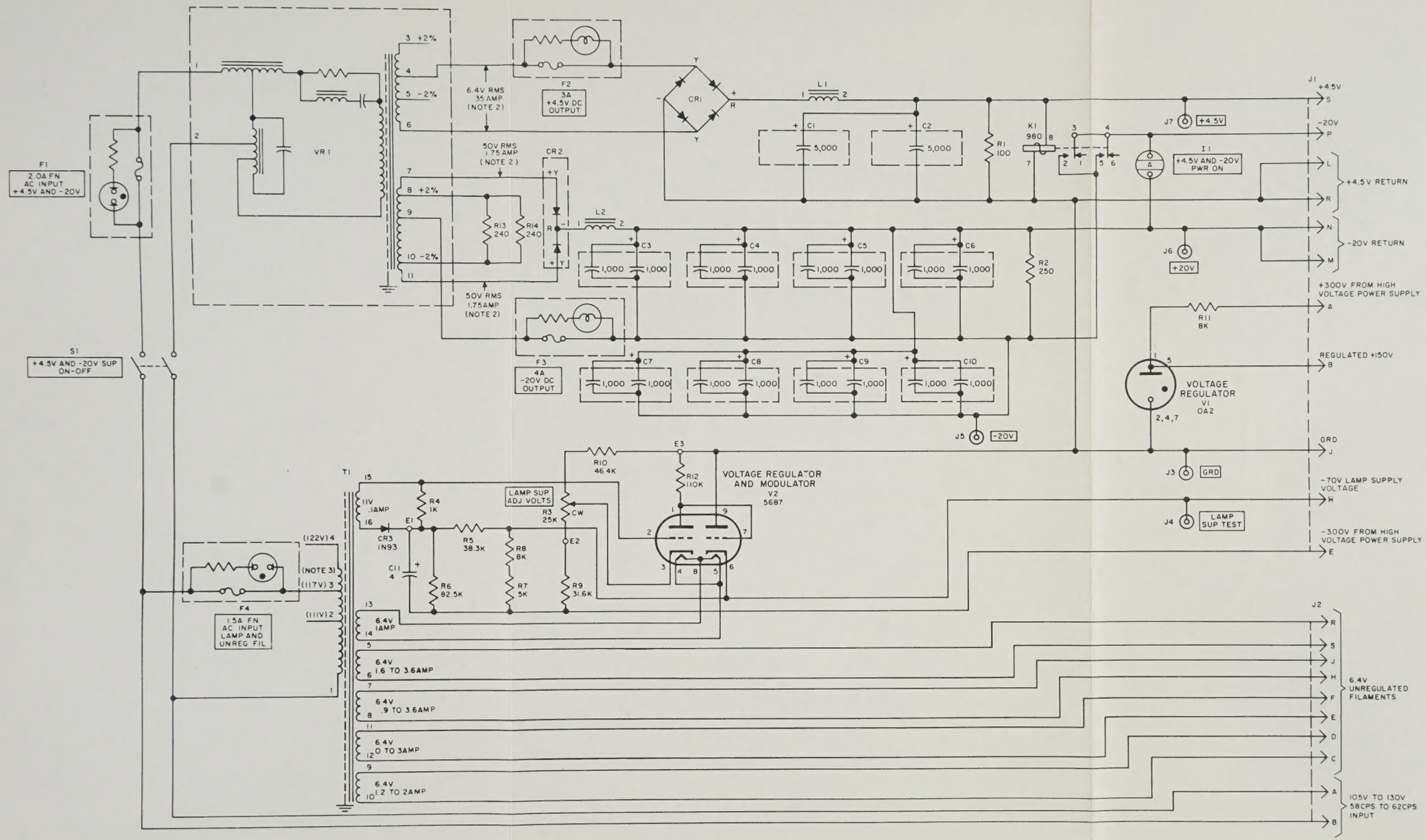


*Figure 180. Electrical test panel SP *6/TSQ-36, wiring diagram.*

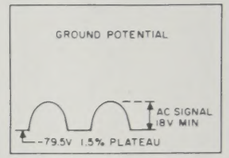
TM 5840-219-35-162

594953 O - 59 (In pocket)

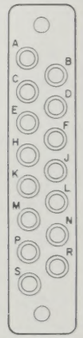


NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. TAPS 3 AND 5 ON (VR1) PROVIDE ±2% ADJUSTMENTS FOR THE +4.5V OUTPUT. TAPS 8 AND 10 PROVIDE A ±2% ADJUSTMENT FOR THE -20V OUTPUT. THESE TAPS ARE SELECTED DURING MANUFACTURE TO MAKE THE -20V TO +4.5V RATIO AS CLOSE TO 4.44 AS POSSIBLE, WHILE MAINTAINING A NOMINAL +4.5V OUTPUT.
3. SELECT TAPS ON TRANSFORMER (T1) NEAREST TO THE NOMINAL LINE VOLTAGE, UNITS WILL BE FURNISHED WIRED TO TAP 3 (117V).
4. ON OUTPUT CONNECTOR (J1) PINS C, D, F, AND K ARE SPARES. ON OUTPUT CONNECTOR (J2) PINS K, L, M, N, AND P ARE SPARES.
5. [ ] INDICATES EQUIPMENT MARKING.
6. ALL RESISTORS ARE ±2% TOLERANCE.



LAMP SUPPLY VOLTAGE CHARACTERISTIC AS VIEWED ON A CALIBRATED OSCILLOSCOPE.



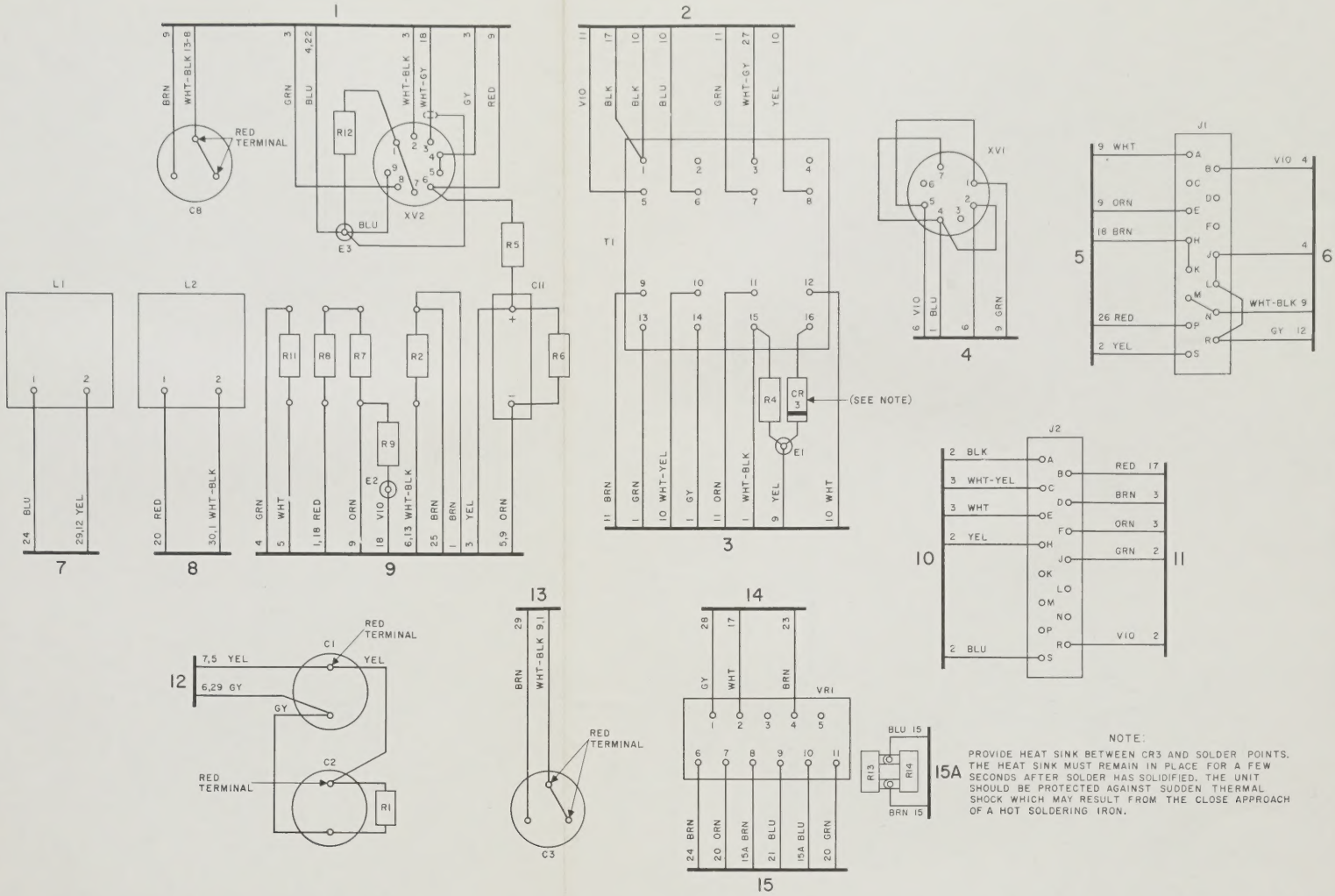
J1 AND J2
WIRING SIDE

HIGHEST REFERENCE DESIGNATIONS		
C11	CR3	R14

Figure 181. Power supply PP-2235/G, schematic.

504953 O - 59 (In pocket)

TM 5840-219-35-165

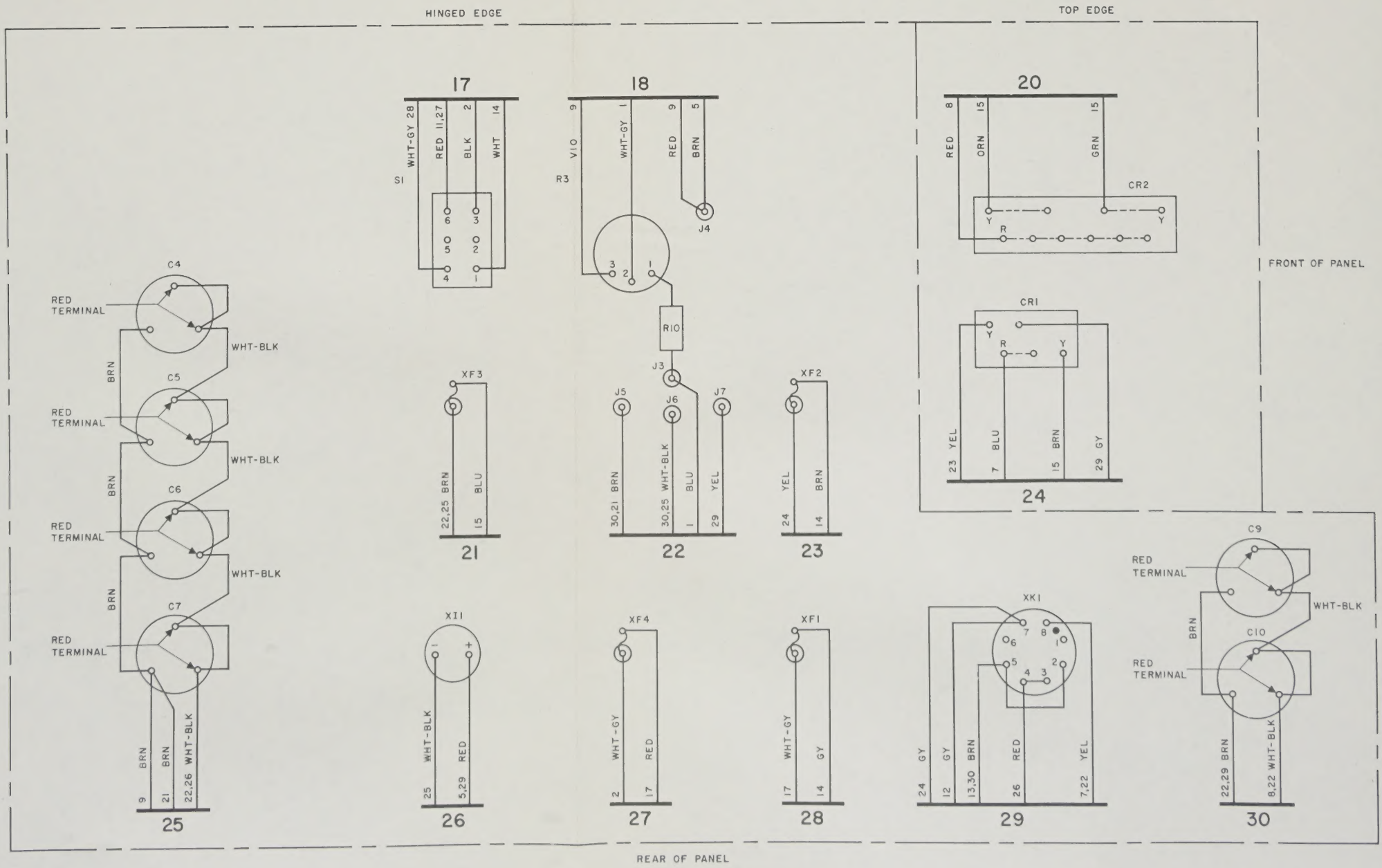


NOTE:

PROVIDE HEAT SINK BETWEEN CR3 AND SOLDER POINTS. THE HEAT SINK MUST REMAIN IN PLACE FOR A FEW SECONDS AFTER SOLDER HAS SOLIDIFIED. THE UNIT SHOULD BE PROTECTED AGAINST SUDDEN THERMAL SHOCK WHICH MAY RESULT FROM THE CLOSE APPROACH OF A HOT SOLDERING IRON.

564953 O - 59 (In pocket)

Figure 182. Power supply PP-2235/G, wiring diagram.



504953 O - 59 (In pocket)

TM 5840-219-35-166 (2)

Figure 182—Continued.

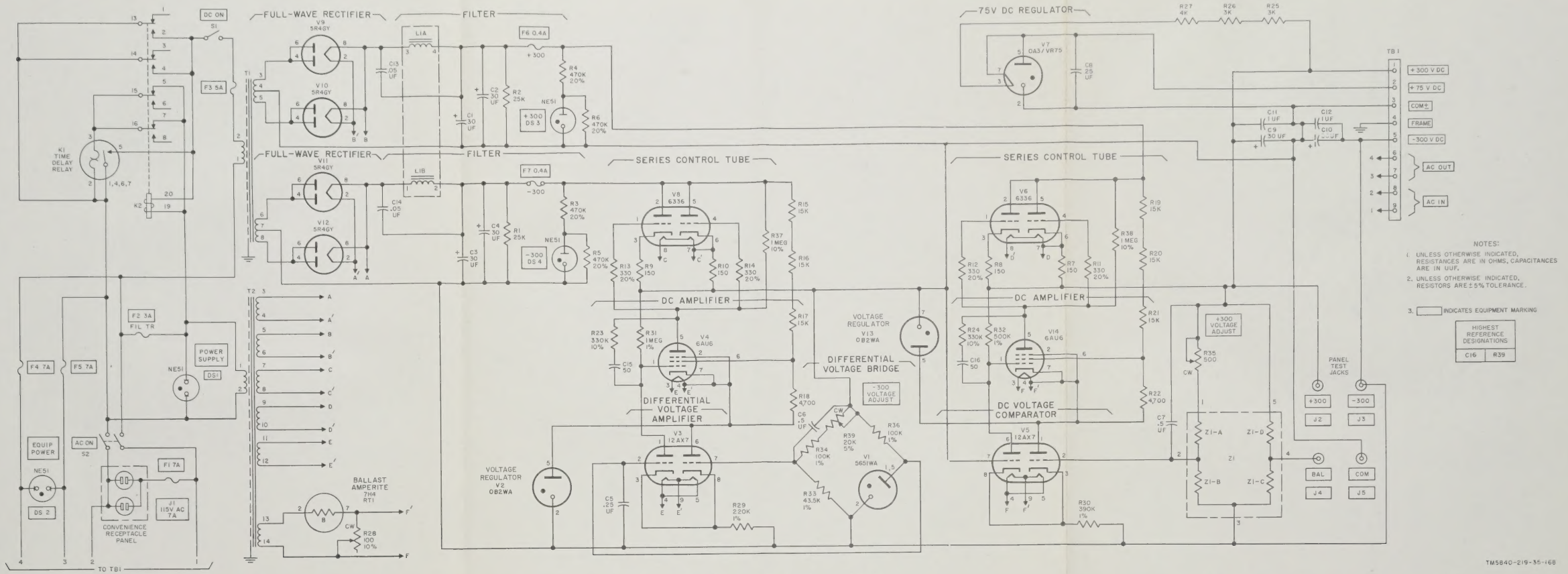
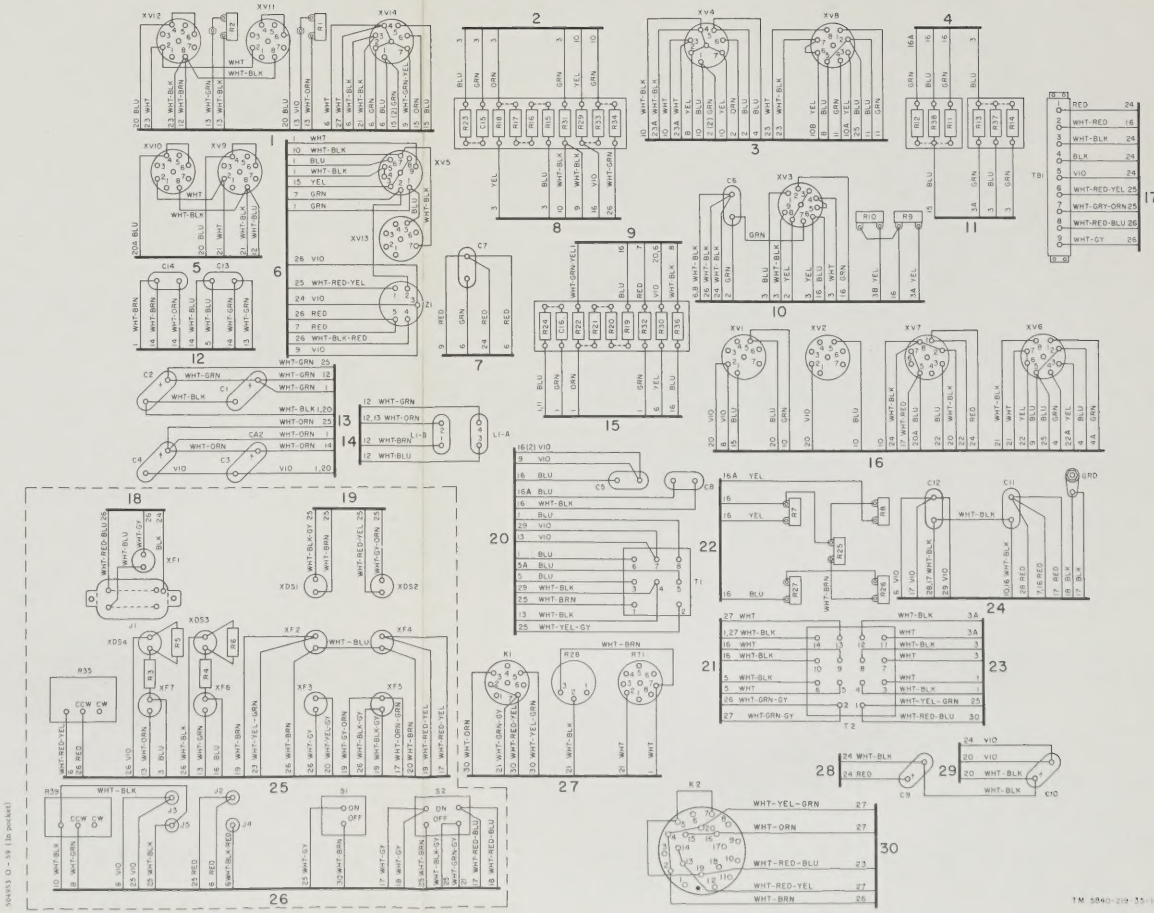
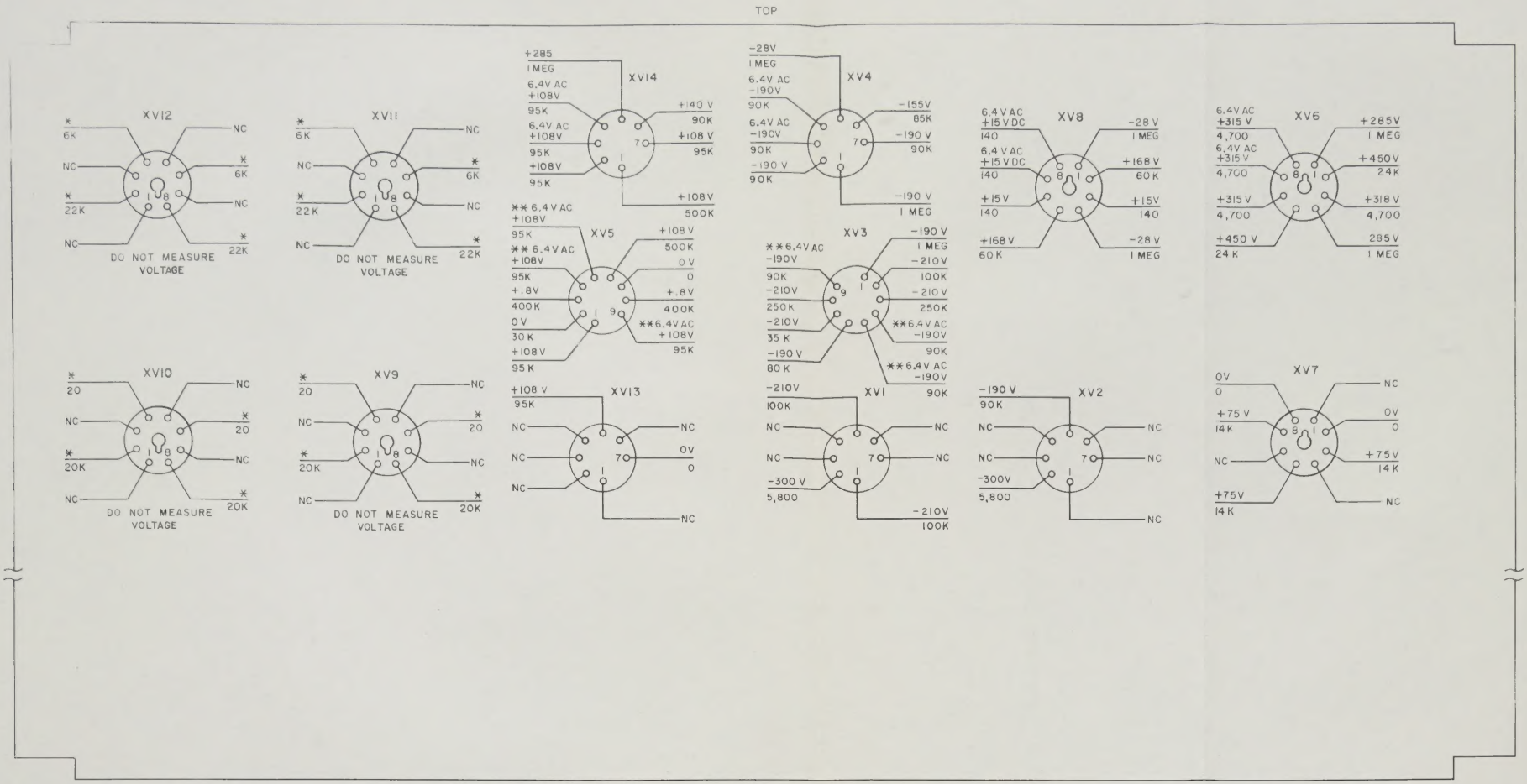


Figure 184. Power supply PP-2236/G, schematic.


XV12
XV11
XV14
XV10
XV9
XV5
XV13
XV4
XV8
XV3
XV1
XV2
XV7
XV6
XF1
XF2
XF3
XF4
XF5
XF6
XF7
XF8
XDS1
XDS2
XDS3
XDS4
J1
J2
J3
J4
J5
S1
S2
K1
K2
T1
T2
TB1
R26
R35
R39
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C1
C2
C3
C4
CA1
CA2
L1-A
L1-B
WHT-BLK
WHT-GRN
WHT-ORN
WHT-BLU
WHT-RED-BLU
WHT-RED-YEL
WHT-GRN-YEL
WHT-BRN
WHT-GY
WHT-YEL-GRN
WHT-RED-BLK
WHT-GRY-ORN
WHT-BLK-GRY
WHT-BLU-GRN
WHT-BLK-RED
WHT-GRN-GY
WHT-YEL-BRN
WHT-RED-GRN
WHT-BLK-ORN
WHT-BLU-GRY
WHT-GRN-BRN
WHT-RED-GRY
WHT-GRY-GRN
WHT-BLK-GRN
WHT-BLU-GRN
WHT-BLK-GRY
WHT-GRN-ORN
WHT-RED-BLU
WHT-RED-YEL
WHT-BRN
WHT-GRN-GY
WHT-YEL-GRN
WHT-RED-BLU
WHT-RED-YEL
WHT-BRN
WHT-ORN
WHT-RED-BLU
WHT-RED-YEL
WHT-BRN
WHT-YEL-GRN
WHT-ORN
WHT-RED-BLU
WHT-RED-YEL
WHT-BRN
WHT-BLK
WHT-BLU
WHT-GRN
WHT-ORN
WHT-RED
WHT-BLK
WHT-GRN
WHT-BLU



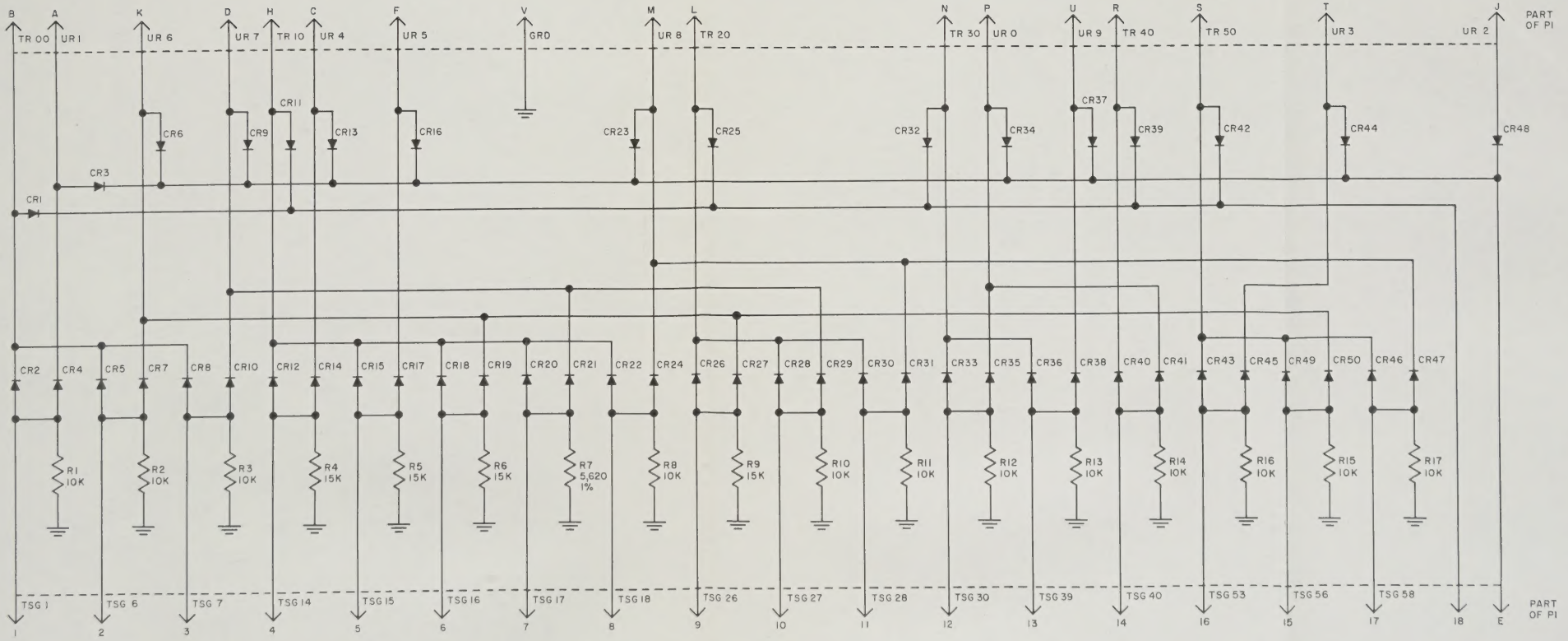
NOTES:

1. DC VOLTAGE MEASUREMENTS MADE WITH 20,000 OHMS PER VOLT METER.
2. RESISTANCES ARE IN OHMS AND ARE MEASURED TO CHASSIS GROUND UNLESS OTHERWISE SPECIFIED.
3. * DO NOT MEASURE VOLTAGE.

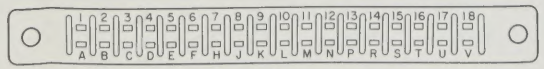
TM5840-219-35-170

504953 O - 59 (In pocket)

Figure 186. Power supply PP–2236/G, voltage and resistance diagram.



T/R PACKAGE



P1
WIRING SIDE

NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE SM-B-181088.
3. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±5% TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.

ABBREVIATIONS:

TR- TENS RING STAGE
TSG-TIME SLOT GATE
UR- UNITS RING STAGE

HIGHEST REFERENCE DESIGNATIONS	
CR50	R17

504953 O - 59 (In pocket)

TM 5840-219-35-171

Figure 187. Transmitter unit subassembly MX-2688/G, schematic.

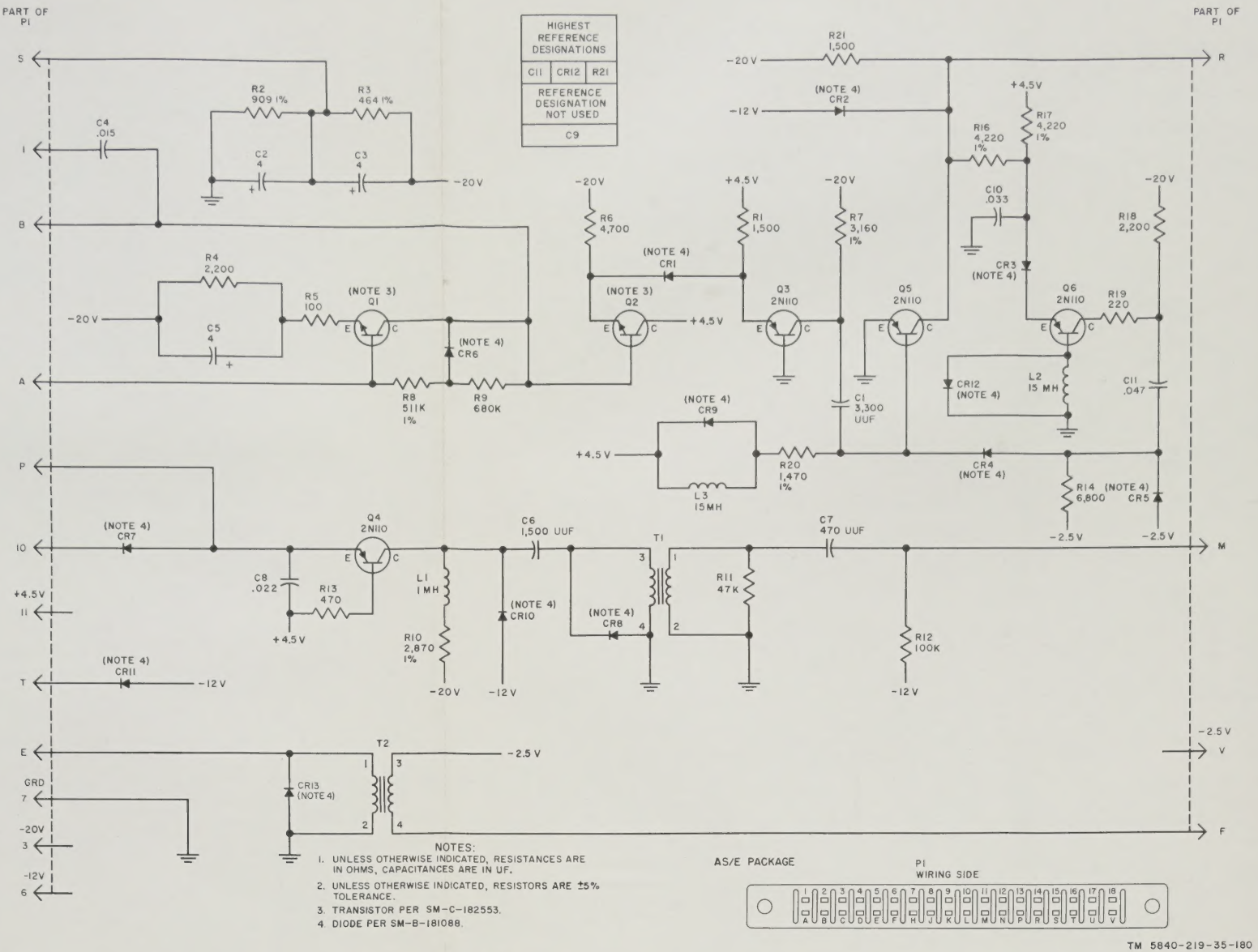
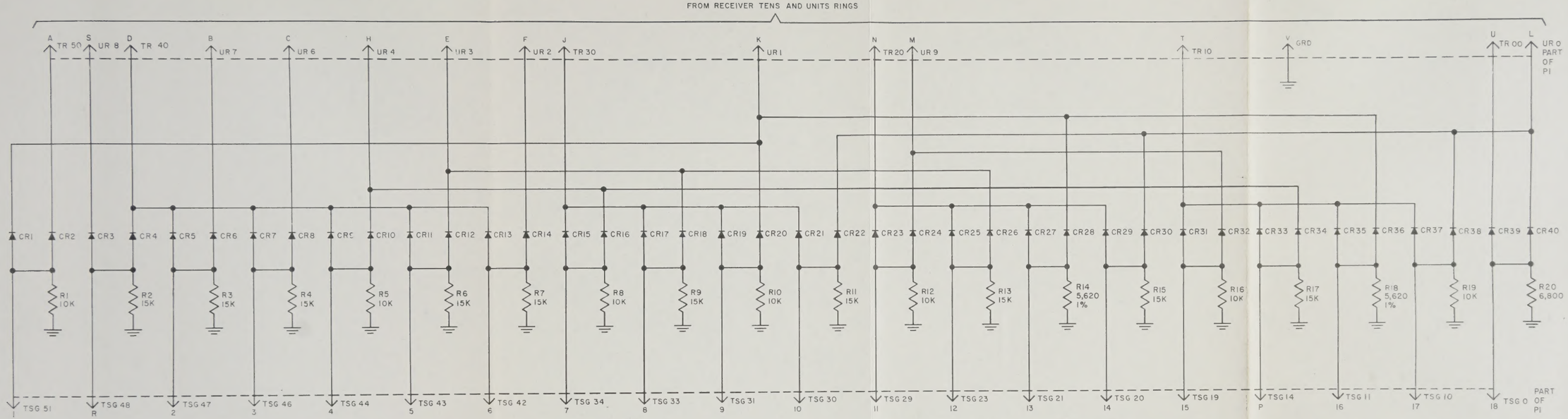


Figure 196. Amplifier-synchronizer unit subassembly MX-2349A/G, schematic.



R/T PACKAGE

NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE ±5% TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
3. ALL DIODES ARE SM-B-181088.

ABBREVIATIONS:
TR – TENS RING STAGE
TSG – TIME SLOT GATE
UR – UNITS RING STAGE

HIGHEST REFERENCE DESIGNATIONS	
CR40	R20

Figure 197. Receiver unit subassembly MX-2685/G, schematic.

384933 O - 59 (to packet)

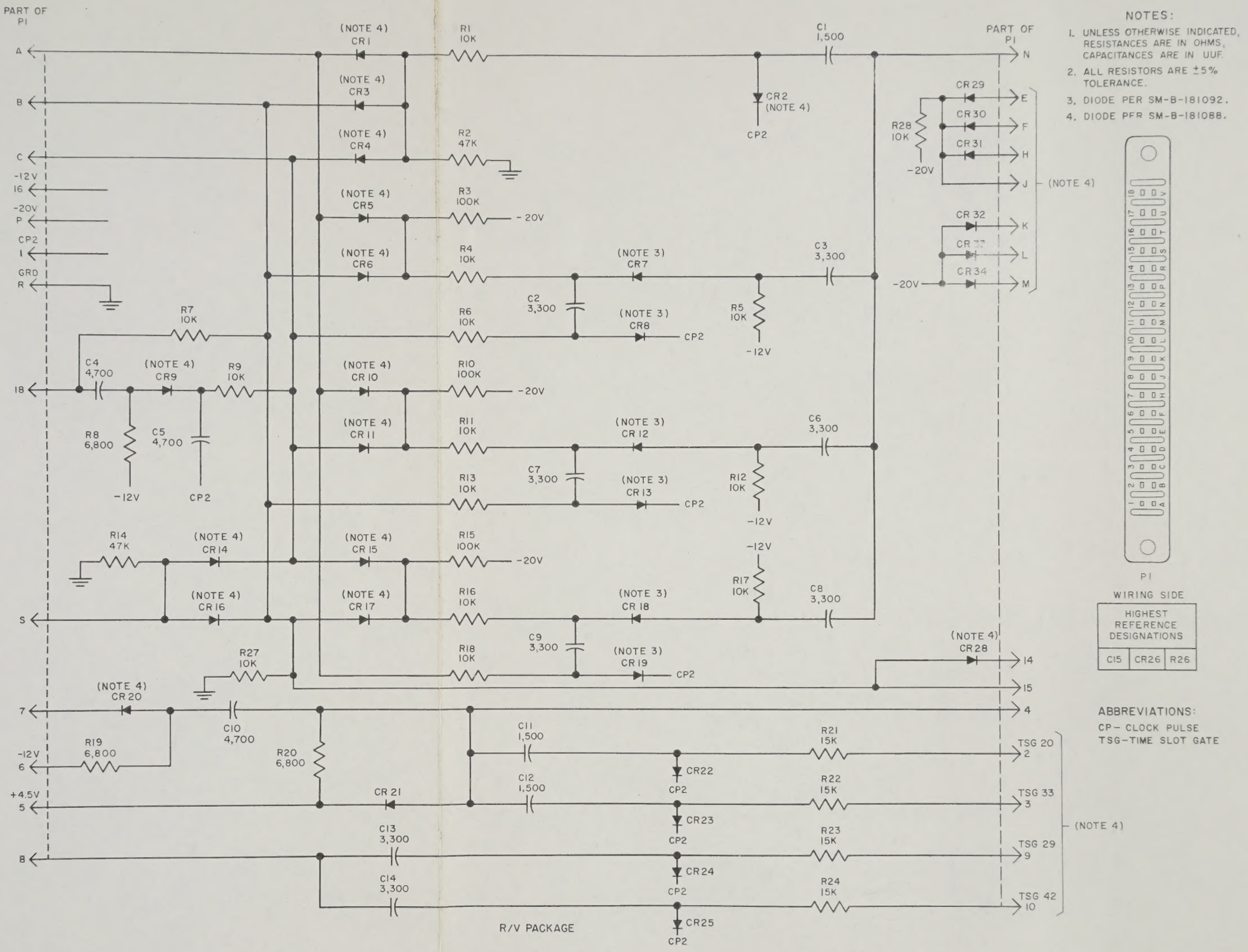


Figure 199. Receiver unit subassembly MX–2686/G, schematic.

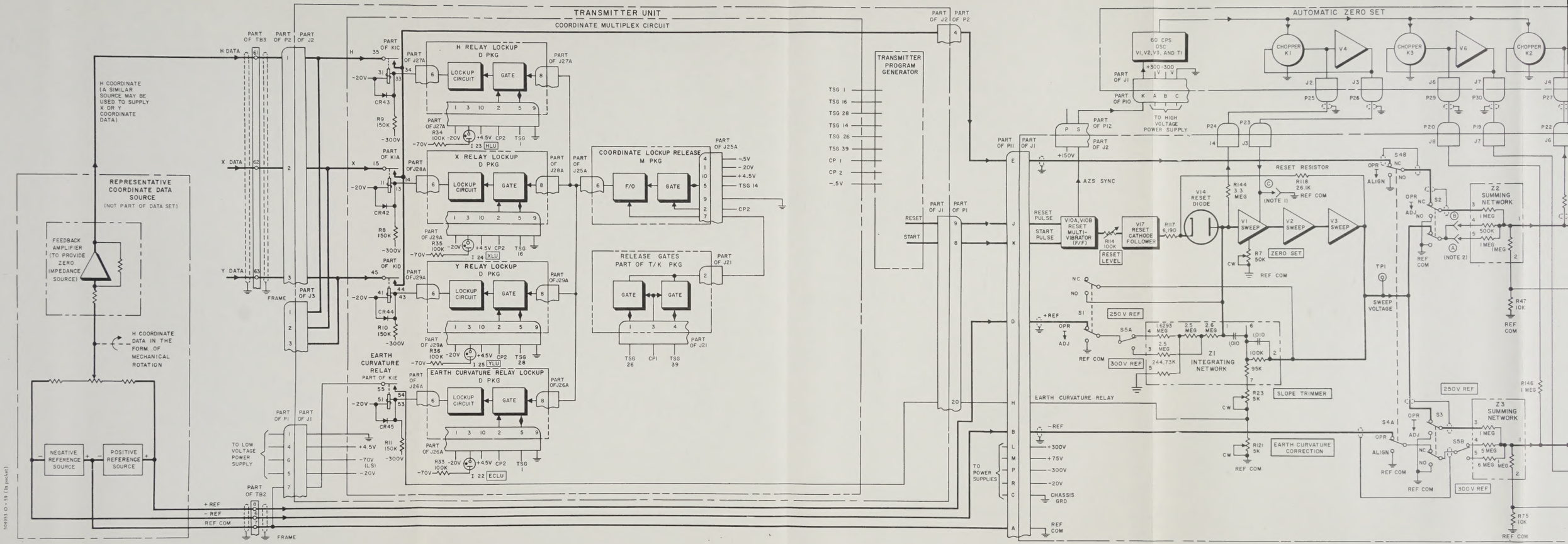


Figure 202. Coordinate multiplexing and encoding, functional schematic.

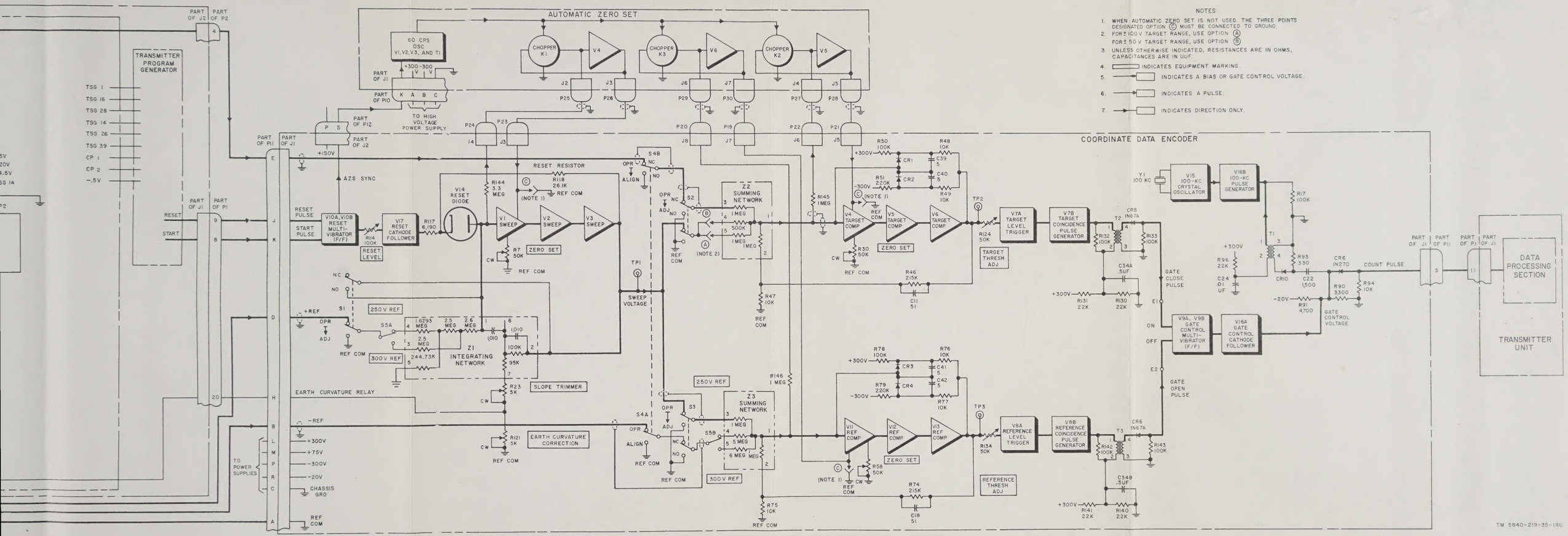


Figure 202. Coordinate multiplexing and encoding, functional schematic.

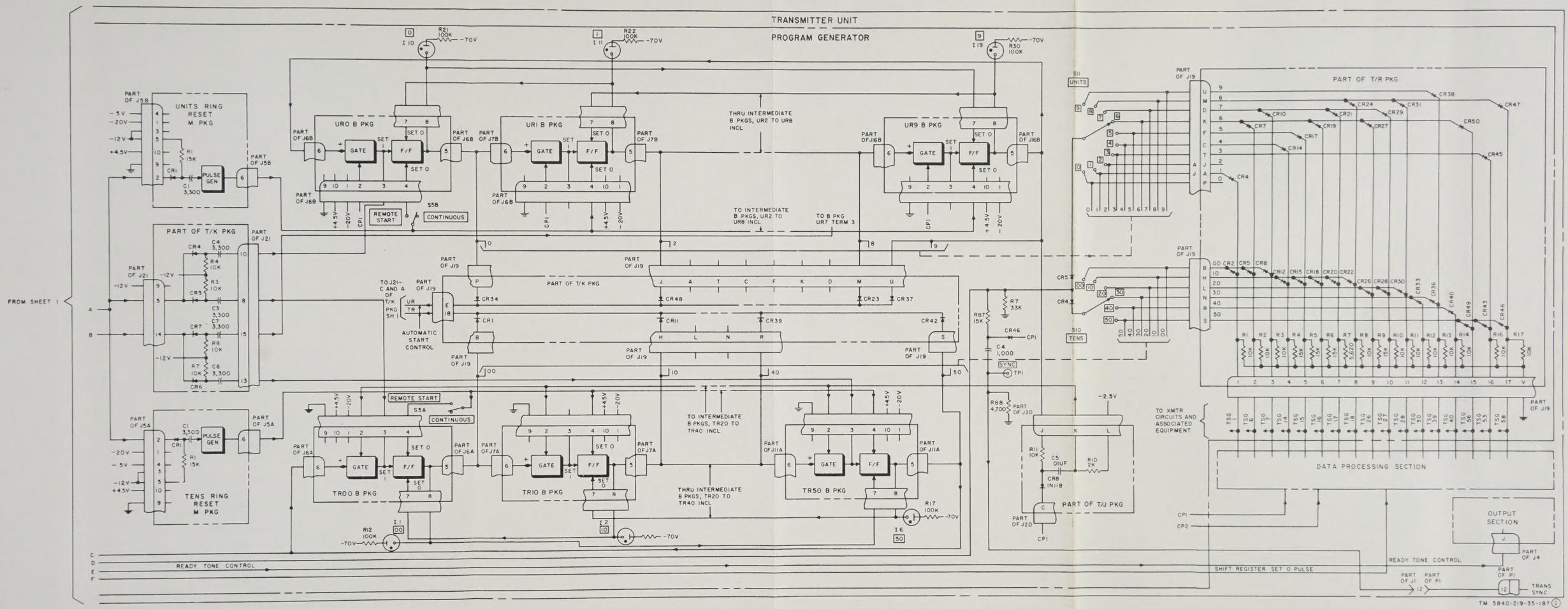


Figure 203—Continued.

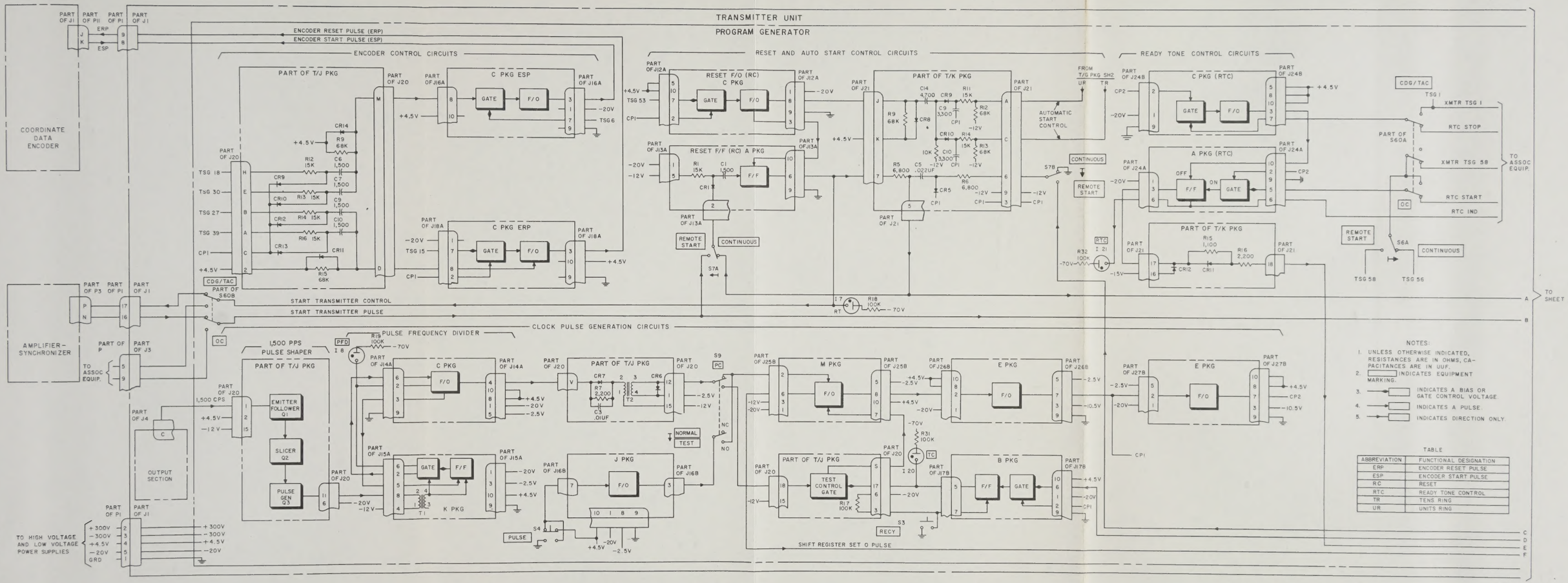


Figure 203. Transmitter program generator, functional schematic.

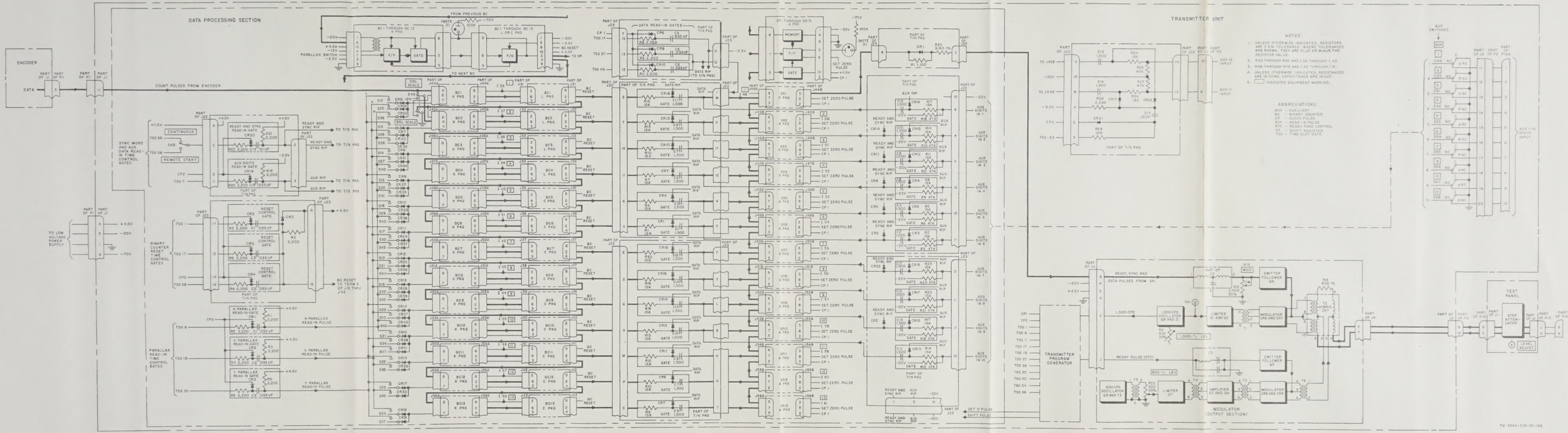

DATA PROCESSING SECTION
TRANSMITTER UNIT
ENCODER
DATA
COUNT PULSES FROM ENCODER
FROM PREVIOUS BC
TO NEXT BC
BC1 THROUGH BC13 X PKG
BC1 THROUGH BC13 L OR C PKG
PARALLAX SWITCH
TO SR
SYNC WORD AND AUX DATA READ-IN TIME CONTROL GATES
CONTINUOUS
REMOTE START
READY AND SYNC READ-IN GATE
AUX DIGITS READ-IN GATE
READY AND SYNC RIP
AUX RIP
TO T/S PKG
TO T/N PKG
BINARY COUNTER RESET TIME CONTROL GATES
RESET CONTROL GATE
BC RESET TO TERM 6 OF J-31 THRU J-43
PARALLAX READ-IN TIME CONTROL GATES
H PARALLAX READ-IN GATE
X PARALLAX READ-IN GATE
Y PARALLAX READ-IN GATE
H PARALLAX READ-IN PULSE
X PARALLAX READ-IN PULSE
Y PARALLAX READ-IN PULSE
TO LOW VOLTAGE POWER SUPPLY
DATA READ-IN GATES
DATA RIP
SET ZERO PULSE
SET 0 PULSE
SHIFT PULSE
TRANSMITTER PROGRAM GENERATOR
READY SYNC AND DATA PULSES FROM SR
1,500-CPS
READY PULSE (RTC)
600-CPS OSCILLATOR Q9 AND Q5
LIMITER Q7
AMPLIFIER Q3 AND Q4
MODULATOR Q6 AND Q8
EMITTER FOLLOWER Q5
MODULATOR (OUTPUT SECTION)
AUX SWITCHES
AUX DIGITS INPUT
TEST PANEL
STEP ATTENUATOR
LEVEL ADJUST
NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTORS ARE 5% TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
2. R53 THROUGH R65 AND 136 THROUGH 149
3. R66 THROUGH R78 AND 150 THROUGH 163
4. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCE ARE IN MFD.
5. [ ] INDICATES EQUIPMENT MARKING.
ABBREVIATIONS:
AUX – AUXILIARY
BC – BINARY COUNTER
CP – CLOCK PULSE
RIP – READ-IN PULSE
RTC – READY TONE CONTROL
SR – SHIFT REGISTER
TSG – TIME SLOT GATE

Figure 204. Transmitter data processing and output, functional schematic.

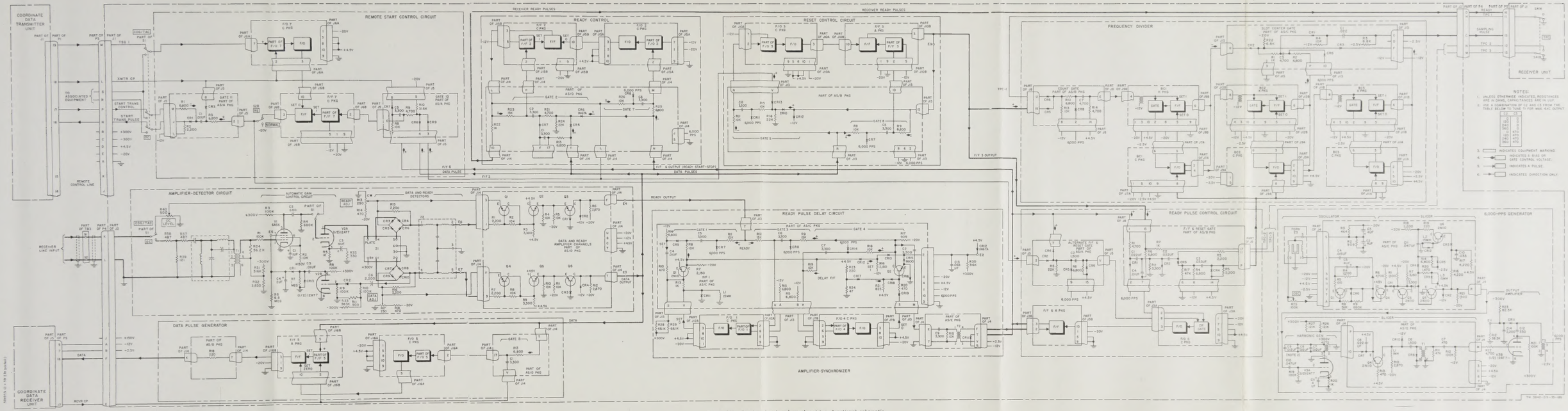

COORDINATE DATA TRANSMITTER UNIT
REMOTE CONTROL LINE
TO ASSOCIATED EQUIPMENT
START TRANS CONTROL
START TRANS PULSE
REMOTE START CONTROL CIRCUIT
READY CONTROL
RESET CONTROL CIRCUIT
RECEIVER READY PULSES
F/F 6 OUTPUT (READY START-STOP DATA PULSE)
DATA PULSE
FREQUENCY DIVIDER
AMPLIFIER-DETECTOR CIRCUIT
AUTOMATIC GAIN CONTROL CIRCUIT
DATA AND READY DETECTORS
DATA AND READY AMPLIFIER CHANNELS PART OF AS/G PKG
READY PULSE DELAY CIRCUIT
READY PULSE CONTROL CIRCUIT
AMPLIFIER-SYNCHRONIZER
DATA PULSE GENERATOR
OSCILLATOR
SLICER
6,000-PPS GENERATOR
OUTPUT AMPLIFIER
RECEIVER LINE INPUT
COORDINATE DATA RECEIVER UNIT
RECEIVER UNIT
NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES 1 OR MF IN UUF.
2. USE A COMBINATION OF C2 AND C5 FROM THE TABLE BELOW TO TUNE T1 FOR MAX. R4C OUTPUT
3. INDICATES EQUIPMENT WARNING
4. INDICATES A GATE OR GATE CONTROL VOLTAGE.
5. INDICATES A PULSE
6. INDICATES DIRECTION ONLY

Figure 265. Receiver input and synchronizing, functional schematic.

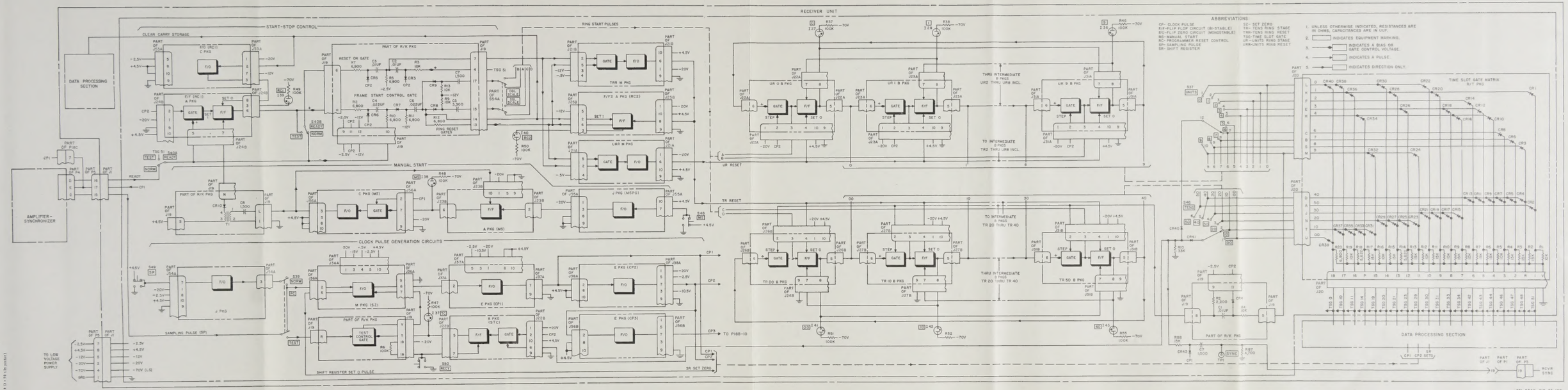


Figure 206. Receiver program generator, functional schematic.

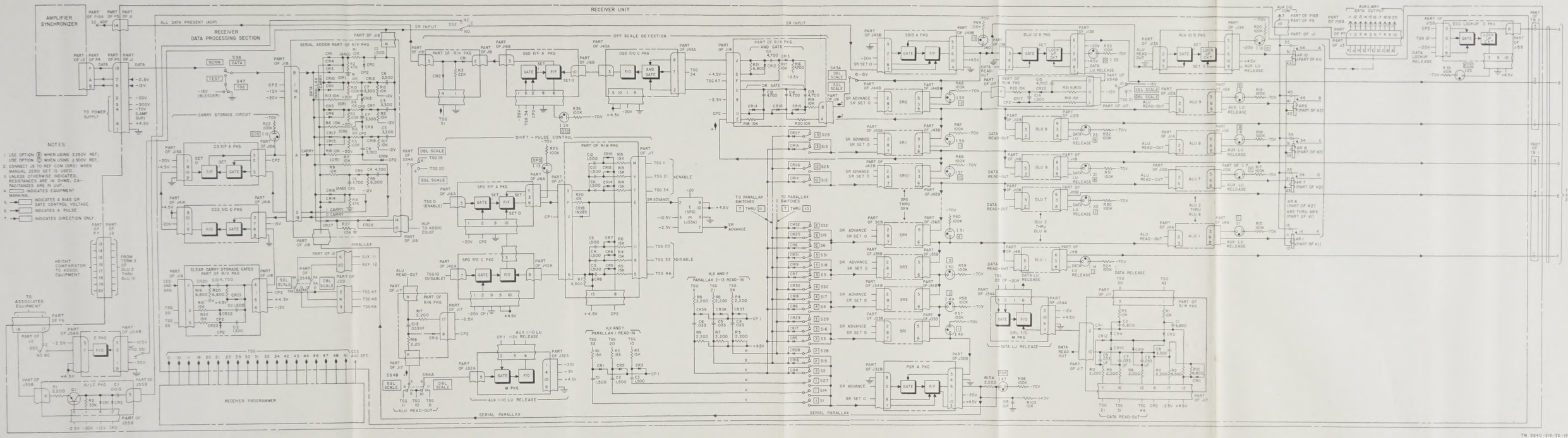

RECEIVER UNIT
AMPLIFIER SYNCHRONIZER
RECEIVER DATA PROCESSING SECTION
ALL DATA PRESENT (ADP)
SR INPUT
OFF SCALE DETECTION
SERIAL ADDER PART OF R/V PKG
CARRY STORAGE CIRCUIT
SHIFT - PULSE CONTROL
CLEAR CARRY STORAGE GATES PART OF R/V PKG
RECEIVER PROGRAMMER
SERIAL PARALLAX
NOTES:
1. USE OPTION B WHEN USING ±250V REF; USE OPTION A WHEN USING ±300V REF.
2. CONNECT J5 TO REF COM (GRD) WHEN MANUAL ZERO SET IS USED.
3. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
4. INDICATES EQUIPMENT MARKING.
5. INDICATES A BIAS OR GATE CONTROL VOLTAGE.
6. INDICATES A PULSE.
7. INDICATES DIRECTION ONLY.
TO ASSOCIATED EQUIPMENT
HEIGHT COMPARATOR TO ASSOC. EQUIPMENT
TO SHEET 2
TM 5840-219-35-191

Figure 267. Receiver data processing, functional schematic.

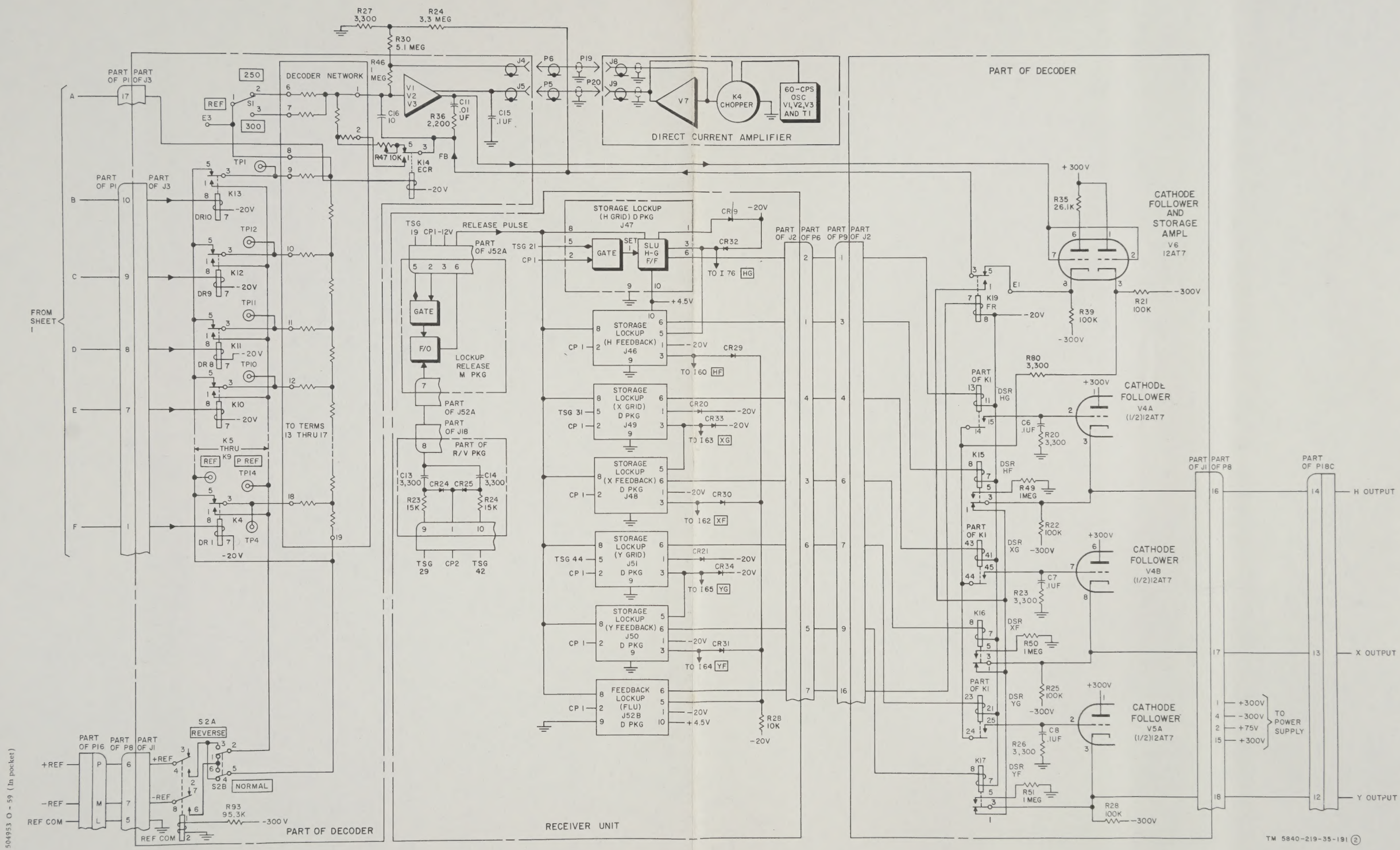


Figure 207—Continued.

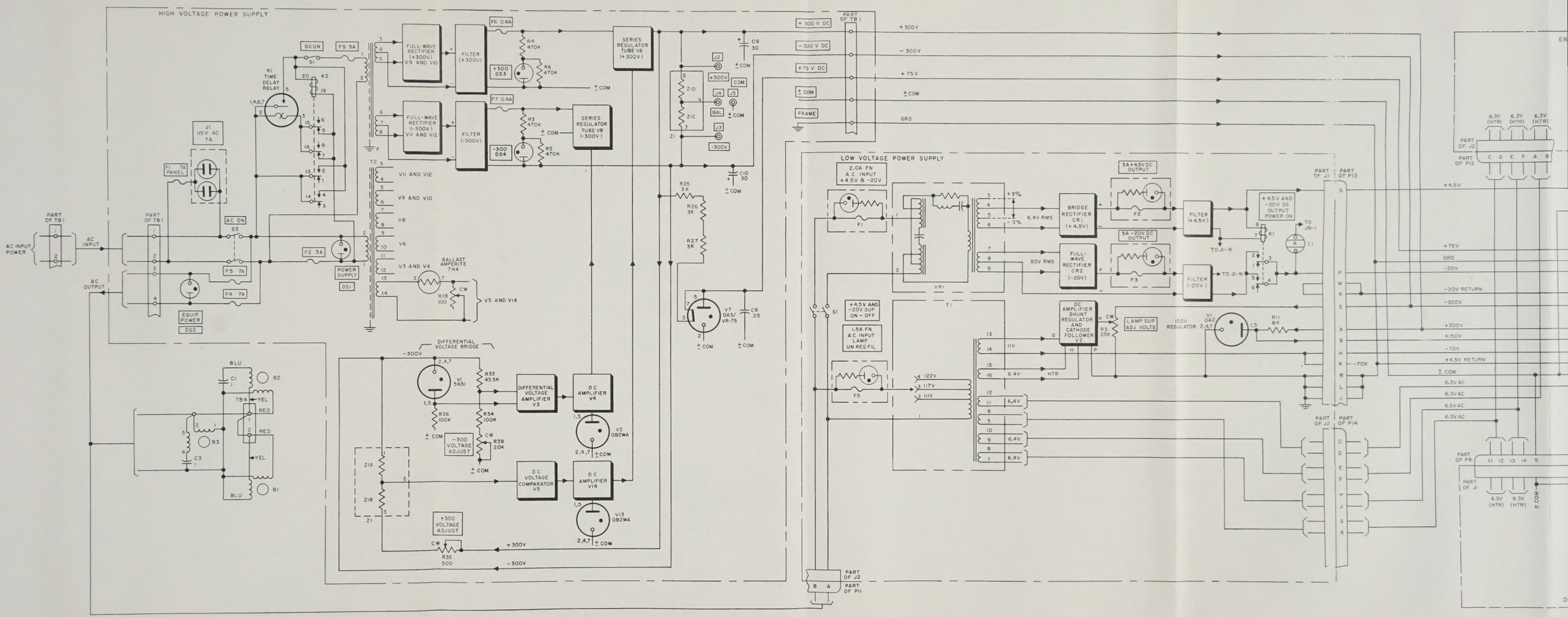


Figure 208. Power supply distribution, functional schematic.

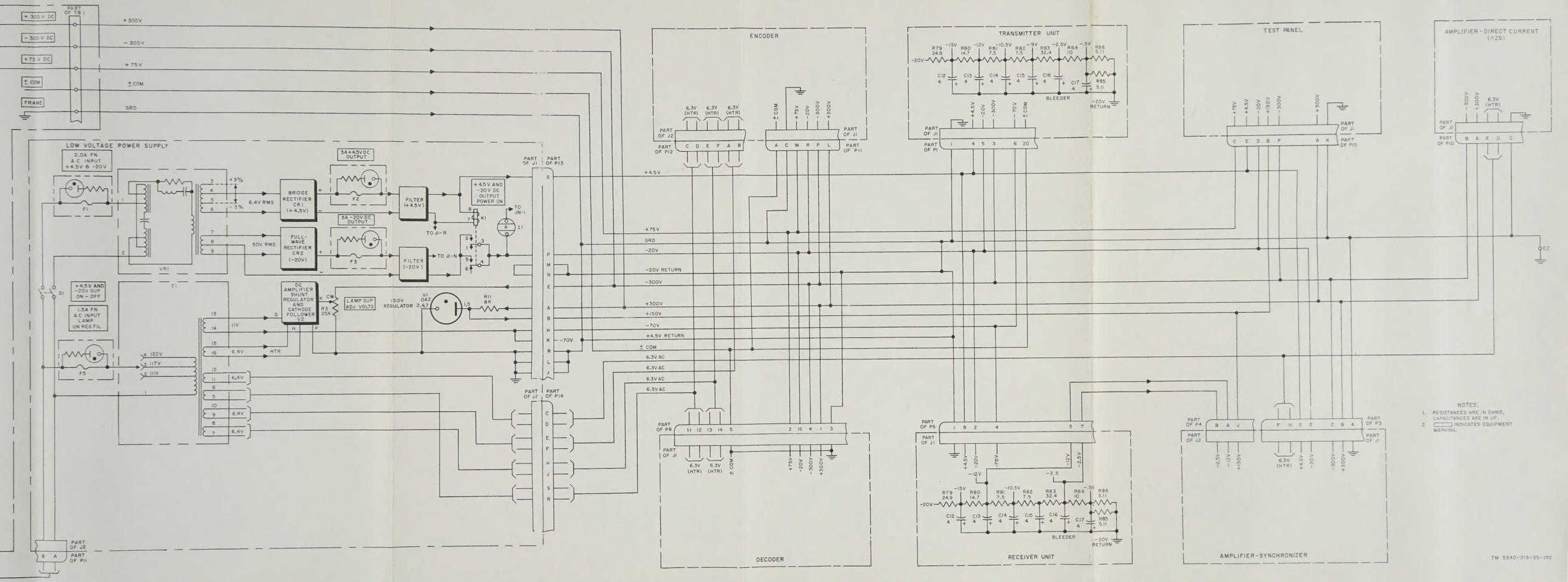


Figure 208. Power supply distribution, functional schematic.

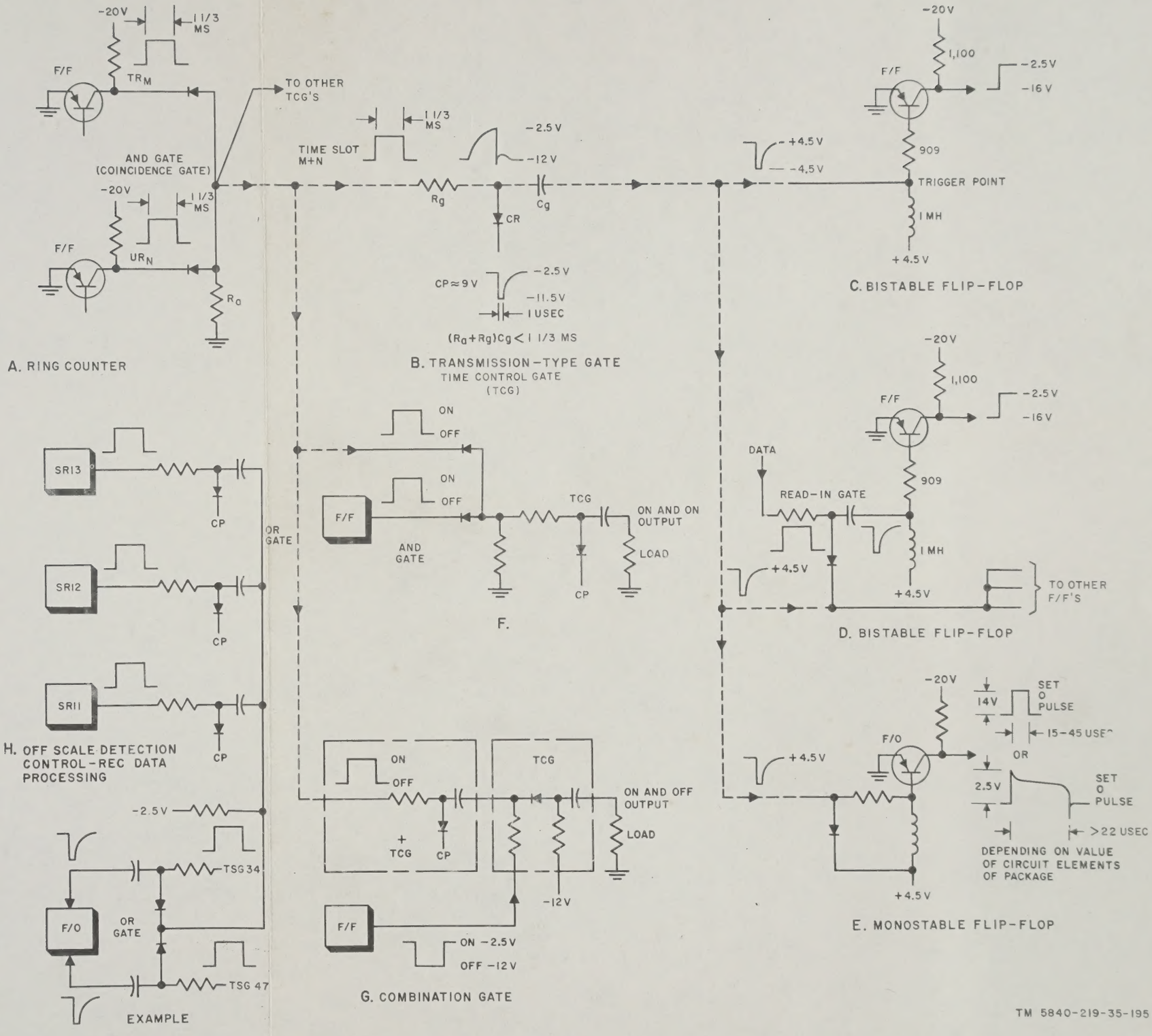


Figure 211. Basic drive and control elements, illustrative circuits.